PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of

CERTAIN FLASH MEMORY CIRCUITS AND PRODUCTS-CONTAINING SAME) Investigation No. 337-TA-382

INITIAL DETERMINATION
Administrative Law Judge Sidney Harris

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Pursuant to the Notice of Investigation, 61 Fed. Reg. 7122-7123 (1996), this is the Administrative Law Judge's Initial Determination in the Matter of Certain Flash Memory Circuits and Products Containing Same, United States International Trade Commission Investigation No. 337-TA-382. 19 C.F.R. § 210.42(a).

The Administrative Law Judge hereby determines that a violation of section 337 of the Tariff Act of 1930, as amended, has been found in the importation and the sale within the United States after importation of certain flash memory circuits and products containing same by reason of infringement of claims 1, 2 and 4 of U.S. Letters Patent 5,418,752 and claim 27 of U.S. Letters Patent 5,172,338.

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I. BACKGROUND

A. Procedural History

By publication in the Federal Register on February 26, 1996, this investigation was instituted pursuant to an Order of the United States International Trade Commission which issued on February 20, 1996, after consideration of a complaint filed on April 21, 1995, on behalf of SanDisk Corp. ("SanDisk"), 3270 Jay Street, Santa Clara, California 95054. See 61 Fed. Reg. 7122-7123 (1996); 19 C.F.R. § 210.10(b).

The Commission's Order required that pursuant to subsection (b) of the Tariff Act of 1930, as amended, an investigation be instituted to determine whether there is a violation of 19 U.S.C. § 1337(a)(1)(B) in the importation into the United States, the sale for importation, or sale within the United States after importation of certain flash memory circuits and products containing same, by reason of infringement of claims 1, 2, 3 or 4 of U.S. Letter Patent 5,418,752 of claims 27, 32 or 44 of U.S. Letters Patents 5,172,338, and whether there exists an industry in the United States as required by subsection (a)(2) of section 337. 61 Fed. Reg. 7123,

The Commission named SanDisk as the Complainant, and the following companies as Respondents:

Samsung Electronic Company, Ltd.
Samsung Main Building, 10th Floor, 250
2-ka Taepyung-Ro Chung-Ku
Seoul, Korea

Samsung Semiconductor, Inc.
3655 North First Street
San Jose, California 95134-1707.

Juan Cockburn, Esq. and William F. Heinze, Esq. of the Office of Unfair Import Investigations ("OUII") were designated as the Commission Investigative Attorneys.

On February 29, 1996, a preliminary conference was held at which SanDisk, Samsung Electronic Company, Ltd. and Samsung Semiconductor, Inc. (collectively, "Samsung"), and OUII were represented. SanDisk, Samsung and OUII remain the only parties in this investigation.[1]

The hearing in this investigation commenced on September 25, 1996, and concluded on October 4, 1996. All parties were represented at the hearing. Post-hearing briefs, and proposed findings of fact and conclusions of law were subsequently filed by all parties.

On September 30, 1996, SanDisk filed its Motion to Strike Testimony and Exclude Evidence Regarding Use of Increment or Decrement of Charge in SanDisk's Flash Memory Devices. Motion Docket No. 382-48.

On October 2, 1996, Samsung filed its Opposition to SanDisk's motion to strike.

Upon consideration of the pleadings filed in connection with the motion to strike, Samsung's pre-hearing filings, and the evidence adduced at the hearing, the Administrative Law Judge has determined that no prejudice occurred which requires the evidence in question to be stricken,

Therefore, SanDisk's Motion No. 382-48 is DENIED.

On October 25, 1996, SanDisk, Samsung and OUII filed supplements to their posthearing briefs and proposed findings of fact. Permission to make supplementary filings was granted during the hearing, and concerned a report prepared by Chipworks, Inc. ("Chipworks"), an independent testing company, which was completed after the hearing. Chipworks tested devices, discussed in detail below, which are alleged by Samsung to invalidate the `338 patent.

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[1] No jurisdictional challenge was made in this investigation. The Administrative Law Judge finds that the Commission has personal jurisdiction over the parties and subject matter jurisdiction over this investigation. See FF I 1-3.

Also on October 25, 1996, Samsung filed a motion entitled Motion for Sanctions Due to SanDisk's Improper *Ex Parte* Contacts with Chipworks, and for a Shortened Response Time. Motion Docket No. 382-49.

On October 31, 1996, SanDisk filed its Opposition to the motion for sanctions.

On November 1, 1996, OUII filed its Response in opposition to the motion for sanctions.

On November 1, 1996, SanDisk filed a supplemental brief in opposition to Samsung's motion for sanctions.

On November 4, 1996, Samsung filed a motion for leave to reply in further support of its motion for sanctions (Motion Docket No. 382-50), and a Reply. Samsung's Motion No. 382-50 to reply is GRANTED.

It appears that both SanDisk and Samsung engaged in contact with Chipworks without the presence of the other parties, and further that there was no agreement concerning contacts with Chipworks. Moreover, based on the pleadings filed in connection with the motion for sanctions it does not appear that the contacts complained of resulted in a material change in Chipwork's Report.

Therefore, Samsung's Motion No. 382-49 for sanctions is DENIED.

On November 7, 1996, Samsung filed its Motion to Strike Complainant's Second Supplemental Proposed Findings of Fact. Motion Docket No. 382-51.

On November 18, 1996, SanDisk filed its Opposition to the motion to strike.

Upon consideration of the pleadings filed in connection with the motion to strike, and the proposed findings in question, the Administrative Law Judge has determined that they are properly filed as proposed rebuttal findings.

Therefore, Samsung's Motion No. 382-51 to strike is DENIED.

Any motions not previously ruled upon are hereby denied.

This Initial Determination is based on the entire record of this proceeding. Proposed findings not herein adopted, either in form or in substance, are rejected as not being supported by the evidence or as involving immaterial matters.

The findings of fact include references to supporting evidentiary items in the record. Such references are intended to serve as guides to the depositions, exhibits, and testimony supporting the findings of fact; they do not necessarily represent complete summaries of the evidence supporting each finding. Some findings of fact are contained only in the opinion.

The following abbreviations are used in this Initial Determination:

CX - Complainant's Exhibit

CPX - Complainant's Physical Exhibit

RX - Respondents' Exhibit

RPX - Respondents' Physical Exhibit

SX - Commission Investigative Staff ("OUII") Exhibit

FF - Finding of Fact

PFF - Proposed FF (CPFF, RPFF, or SPFF)

PRFF - Proposed Reply FF

Dep. - Deposition

Tr. - Transcript.

B. Technological Background

This investigation concerns flash EEPROMs. An EEPROM, or E^2PROM (a so-called "E-squared prom"), is an electrically erasable programmable read only

memory. FF I 8, 9. EEPROMS, EPROMs[2] and hard disk mechanical memories are examples of "nonvolatile" memories because they retain information even when their power is off.[3] The term "flash" in "flash EEPROM" refers to the quick speed of the erasing operation. FF I 12.

In a flash EEPROM, the flash memory cells are transistors, each of which has a source, a gate and a drain. FF I 13, 14. The gate has a "floating gate," which consists of a metal or conducting region that lies between the substrate of the cell and what is called the control gate. The floating gate floats in an oxide insulator. FF I 15. The source and the drain are electron-enriched regions located on the substrate of the cell on either side of the gate. FF I 16.

In each transistor, a positive voltage must be placed on the gate for it to attract electrons, which come from all over the device, through a channel running from the source to the region under the gate and then to the drain. This is the "unprogrammed" state of the cell. FF I 25. A cell is said to be "programmed" when there is a negative charge on the floating gate, which repels electrons, and makes it harder for current to flow from the source to the drain. FF I 25.

If the transistor is "on," current will be conducted across the transistor through the channel from the source to the drain. If the transistor is "off," current will not be conducted across the transistor. FF I 23.

Thus, a memory cell in an EEPROM may operate in a binary system in which

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[2] EPROM is an acronym for electrically programmable read only memory. FF I 6. An EPROM can be erased by exposure to ultraviolet light. FF I 7.

[3] In contrast, volatile RAM ("random access memory") technologies like that used in the SRAM ("static RAM") and DRAM ("dynamic RAM") require a continuous supply of power in order to preserve information. FF I 10.

current flows or does not flow through the cell. FF I 24. Depending on whether a transistor is on or off, it may be said to store a 0 (zero) or a 1. FF I 24. Either state may be called 0 or 1, as long as the use of the terms is consistent. FF I 24.

There are two ways of getting electrons from the substrate to the floating gate in order to program the cell and prevent the flow of current across the cell. FF I 17. One method is hot electron injection (or "HEI"), and the other is Fowler-Nordheim tunneling or programming. Fowler-Nordheim techniques are also used for erasure. FF I 18-22.

The HEI method places a voltage on the control gate which is located above the floating gate. The control gate provides a means of accessing the transistor for reading and programming. There is no contact between the floating gate and the control gate except through capacitance. However, to program a transistor a high electric field or voltage such as 7 volts is applied to the drain, zero volts is applied to the source, and 12 volts is applied to the control gate. The electrons are thus accelerated to the point at which some of them cross the oxide around the floating gate to be captured on the floating gate. The electrons will generally remain there until they are removed. FF I 18.

To erase a cell that has been programmed using the HEI method, one uses Fowler-Nordheim tunneling, which is based on a quantum mechanical phenomenon. One may reverse the electric field and cause the electrons to move in the direction opposite to the way they would move if Fowler-Nordheim programming had been used. FF I 19.

In Fowler-Nordheim programming, a very high voltage to the gate of the device brings electrons close to the surface and increases the probability of being able to measure electrons in the floating gate. The technique relies on

the tunneling of electrons through material which is normally thought of as an insulator. When the high voltage is taken off, electrons are stuck on the floating gate. The presence of the electrons on the floating gate affects the flow of current from source to drain. FF I 20.

To erase using a Fowler-Nordheim technique with devices that were built for Fowler-Nordheim programming, and do not have thick oxide layers, one simply reverses the voltages to effect erasure. Electrons tunnel from the substrate to the gate or from the gate to the substrate depending on whether one wishes to program or erase. FF I 21. To erase using the a Fowler-Nordheim technique with devices that were not built for Fowler-Nordheim programming, and which have thick oxide and for which one has used HEI programming, one uses a dedicated electrode for erasing. The electrode may be placed in various regions, for example, on the side of the floating gate, or overlapping the floating gate. The electrode acts to remove the electrons from the floating gate. FF I 22.

There are various methods of reading a cell to determine whether it is programmed (with no current flowing through it) or unprogrammed. FF I 26.

One could read a cell with a sense amplifier in which the current is compared with the current that one would expect to flow in a cell that is not programmed. The actual current that would flow through a cell is very small. If the sense amplifier senses current, it compares that current, and then creates a large output signal. Thus it is called a "sense amplifier." FF I 27.

Another method of reading a cell is simply to determine whether current flows or not, in contrast to comparing the current against another signal. FF I 28.

EEPROM cells can also be used for multistate storage, or multilevel

storage, in which rather than reading a cell as merely on or off -- unprogrammed or programmed -- a cell has additional individual states. Instead of each cell having a zero and a one, which constitutes one bit of information, a cell can have two, three, four or more bits. FF I 29.

Multistate storage requires very precise and accurate programming to the various individual states. Multistate devices are not currently in commercial use. FF I 30.

There are a number of ways of connecting the memory cells in an EEPROM, typical among them are NOR (which is used by SanDisk), and NAND (which is used by Samsung). FF I 32, 34.

With the NOR[4] connection, there are three connections to each cell. One can thus have independent control of the source, the drain or the gate with any of the cells. FF I 37. If, for example, three cells A, B and C are connected in a row as NOR cells,[5] and there is one line to put current in, and another line to determine whether there is current out, a sense amplifier or other device will indicate that there is current out if just one of the cells A, B or C acts as a closed switch. FF I 37.

With the NAND connection,[6] the cells are connected in series. One can make the source of one cell equal to the drain of the another cell. Current will flow to the output only if all the cells (for example, A, B, C and so on) are closed. FF I 38.

NAND cells take up less space that NOR cells. FF I 39. With NAND

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[4] NOR derives from standard logic terminology, and stands for "not or," an inverted OR signal. FF I 36.

[5] Currently, commercial flash EEPROMs have millions of cells, e.g., 16 or 32 million. FF I 41.

[6] NAND derives from the standard logic terminology "not and." FF I 38.

connections, one does not have to access the individual nodes as with NOR connections. However, one does not have individual control of each NAND cell. Therefore, one programs NOR and NAND cells differently. FF I 40.

Flash memory circuits are typically attached to a circuit board with other circuitry and are often contained within a sealed enclosure which is then attached to or installed within a particular application. FF I 42.

A controller is used to address an array of flash memory chips. FF I 43. A controller can be used with flash chips to mimic (or emulate) a disk drive.[7] FF I 43.

Flash EEPROMs use less power than other memory products such as disk drives, and they have no mechanical moving parts and are consequently more rugged. FF I 45. However, there are concerns associated with flash EEPROMs.

Endurance, or fatigue, is a consideration associated with EPROM and EEPROM semiconductor technology because programming and erasing operations cause electrons to become trapped in, and permanently damage, the silicon dioxide (i.e., glass) layer surrounding the floating gate. FF I 46. The resulting fatigue causes the voltage "window" between the erased and programmed states to close before the device ultimately fails. FF I 46.

In the `338 patent, fatigue was addressed at the chip level through individually erasing only selected sectors of the array and through inhibiting further programming of verified cells. FF I 47. Other approaches to maximizing the endurance of flash EEPROM at the controller, or system, level included wear-out leveling, dynamic mapping of defective cells, and error correcting codes. FF I 47.

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[7] Instead of using a hardware controller, some companies use software that tells the host microprocessor how to address the flash memory chips. FF I 44.

Fatigue and other characteristics of using flash EEPROMs are the subject matter of the patents-in-suit.

II. IMPORTATION AND SALE

The Samsung Respondents have imported or are importing at least the following products into the United States: [

[C]

] FF II 1

Respondents are selling or have sold at least the following products after such products have been imported into the United States: [

[C]

] FF II 2.

[

[C]

] FF II 5.

Respondents have not provided any documentary evidence that they are importing [[C]

] It has not been established that these devices have been imported into the United States.[8]

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[8] [

[C]

(continued...)

III. CLAIM CONSTRUCTION

Complainant SanDisk asserts that Samsung infringes claims 1, 2 and 4 of the `752 patent, and claim 27 of the `338 patent.[9] Complainant also argues in satisfaction of the domestic industry requirement that it practices claims 1, 2 and 4 of the `752 patent and claim 27 of the `338 patent. Consequently, the proper constructions of claims 1, 2 and 4 of the `752 patent, and claim 27 of the `338 patent are discussed below.[10]

A. General Law of Claim Construction

The construction of patent claims is a matter of law. Markman v. Westview Instruments, Inc., 52 F.3d 967, 979 (Fed. Cir. 1995)(en banc), aff'd, 116 S.Ct. 1384 (1996); Tandon Corp. v. Int'l Trade Comm'n, 831 F.2d 1017, 1021 (Fed. Cir. 1987).

All elements of a patent claim are material, with no single part of a

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[8](...continued)

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Choi, Tr. 1395-1396; see Respondents' Proposed Reply FF 10-12.

[9] As indicated, supra, in the Background section, this investigation was originally instituted to determine whether there is a violation of section 337 in connection with claims 1, 2, 3 or 4 of the `752 patent, or claims 27, 32 or 44 of the `338 patent. Complainant SanDisk has abandoned its contentions regarding claim 3 of the `752 patent, and claims 32 and 44 of the `338 patent. Subsequent to the filing of its complaint, Complainant withdrew its contentions that Samsung infringed claim 3 of the `752 patent and claim 44 of the `338 patent. See CPFF 14 (citing RX 154C at 2). At the hearing, Complainant did not present evidence specifically with respect to claim 32 of the `338 patent. See Respondents' Post-Hearing Br. at 1. Furthermore, claim 32 of the `338 patent was not asserted against Respondents in Complainant's Post-Hearing Brief and Proposed Findings of Fact and Conclusions of Law. See, e.g., Complainant's Proposed Conclusions of Law 135-138. Claim 32 of the `338 patent appears on general inspection to be closely similar to claim 27. Claim 32 is not construed herein, nor are validity and infringement findings made with respect to claim 32.

[10] In order to perform a patent infringement analysis, any claim must first be construed to determine its proper scope and meaning. Palumbo v. Don-Joy Co., 762 F.2d 969, 974 (Fed. Cir. 1985); Lemelson v. General Mills, Inc, 968 F.2d 1202, 1206 (Fed. Cir. 1992), cert. denied, 506 U.S. 1053, 113 S.Ct. 976 (1993).

Co., 54 F.3d 1570, 1576 (Fed. Cir. 1995).

Extrinsic evidence may also be used to construe patent claims. Such evidence "consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." Markman, 52 F.3d at 980. Extrinsic evidence may, for example, help to explain scientific principles, technical terms, or the state of the art at the time of the invention. Id.

A "court may, in its discretion, receive extrinsic evidence in order `to aid the court in coming to a correct conclusion' as to the `true meaning of the language employed' in the patent." Id. (quoting Seymour v. Osborne, 78 U.S. (11 Wall.) 516, 546 (1871)). A trial judge has sole discretion to decide whether or not he needs, or desires, an expert's assistance to understand a patent. Markman, 52 F.3d at 981 (quoting Seattle Box Co. v. Industrial Crating & Packing, Inc., 731 F.2d 818, 826 (Fed. Cir. 1984)). Extrinsic evidence is to be used to understand the patent, not to vary or contradict the terms of the claims.[11] 52 F.3d at 981.

Claim 1 of the `752 patent and claim 27 of the `338 patent contain means-plus-function elements. Therefore, these claims must be construed in view of 35 U.S.C. §112, ¶ 6.[12]

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[11] Extrinsic evidence "may be necessary to inform the court about the language in which the patent is written. But this evidence is not for the purpose of clarifying ambiguity in claim terminology." Markman, 52 F.3d at 986.

[12] 35 U.S.C. § 112, ¶ 6, provides as follows:

> An element in a claim for a combination may be expressed as a means or step for performing a specified function without recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material or acts

(continued...)

claim being more important or "essential" than another. Markman, 52 F.3d at 988.

Claims should be construed as one of ordinary skill in the art would construe them. SmithKline Diagnostics, Inc. v. Helena Laboratories Corp., 859 F.2d 878, 882 (Fed. Cir. 1988).

Nevertheless, "[c]laims must be read in view of the specification, of which they are a part." Markman, 52 F.3d at 979 (quoting Autogiro Co. v. United States, 384 F.2d 391, 197 (Ct. Cl. 1967)). The specification may serve as a sort of dictionary which explains the invention and may define terms used in the claims. 52 F.3d at 979. In fact, it has often been said that "a patentee is free to be his own lexicographer." Id. at 980 (quoting Autogiro, 384 F.2d at 397). However, "any special definition given to a word must be clearly defined in the specification." 52 F.3d at 980 (citing Intellicall, Inc. v. Phonometrics, Inc., 952 F.2d 1384, 1388 (Fed. Cir. 1992)).

In considering the claims in view of the specification, it must be remembered that "[t]he written description part of the specification itself does not delimit the right to exclude. That is the function and purpose of the claims." Markman, 52 F.3d at 980.

To construe claim language, one "should also consider the patent's prosecution history, if it is in evidence." Id. Indeed, the prosecution history (or "file wrapper") "is of primary importance in understanding the claims." Id. Although the prosecution history should be used to understand the language of the claims, like the specification, it cannot enlarge, diminish or vary the claims. Markman, 52 F.3d at 980 (quoting Goodyear Dental Vulcanite, 102 U.S. 222, 227 (1880)). The prosecution history "limits the interpretation of claim terms so as to exclude any interpretation that was disclaimed during prosecution." Southwall Technologies, Inc. v. Cardinal IG

The scope of a means-plus-function claim is confined to structures expressly disclosed in the specification and corresponding equivalents. "Thus, the statutory provision prevents an overly broad claim construction by requiring reference to the specification, and at the same time precludes an overly narrow construction that would restrict coverage solely to those means expressly disclosed in the specification." Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 1569, 1575 (Fed. Cir. 1991)(emphasis in original).

One must "construe the functional claim language `to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.'" Valmont Indus., Inc. v. Reinke Mfg. Co., Inc., 983 F.2d 1039, 1042 (Fed. Cir. 1993)(quoting 35 U.S.C. 112, ¶ 6). Accord In re Donaldson Co., Inc., 16 F.3d 1189, 1193 (Fed. Cir. 1994); In re Bond, 910 F.2d 831, 833 (Fed. Cir. 1990).

In Valmont, the Federal Circuit stated that use of the term "equivalent" in section 112 should not be viewed the same as the doctrine of equivalents which is used in infringement analyses. Nevertheless, the Federal Circuit explained the meaning of "equivalent" as used in section 112, as follows:

> The word 'equivalent' in section 112 invokes the familiar concept of an insubstantial change which adds nothing of significance. In the context of section 112, however, an equivalent results from an insubstantial change which adds nothing of significance to the structure, material or acts disclosed in the patent specification. A determination of equivalence under section 112 does not involve the equitable tripartite test of the doctrine of equivalents. As this court has stated, 'the sole question' under section 112 involves comparison of the structure in the accused device which performs the claimed function to the structure in the specification.

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[12](...continued)
described in the specification and equivalents thereof.

983 F.2d at 1043 (citations omitted).[13]

B. Claims 1, 2 and 4 of the '752 Patent

1. Claim 1

Claim 1 of the '752 patent is as follows:

> A Flash EEprom system comprising:
>
> one or more integrated circuit chips each having an array of Flash EEprom cells partitioned into a plurality of sectors, each sector addressable for erase such that all cells therein are erasable simultaneously;
>
> means for selecting a plurality of sectors among the one or more chips for erase operation;
>
> means for simultaneously performing the erase operation on only the plurality of selected sectors; and
>
> individual register associated with each sector for holding a status to indicate whether the sector is selected or not.

CX 1 ('752 Patent) at col. 16, line 59 through col. 17, line 3.

(a) The Preamble.

The dispute between the parties with respect to the preamble of claim 1 concerns the question of whether or not a "Flash EEPROM System," as that term is used in the preamble, requires a controller.

Claim preambles are construed in a manner that is consistent with the principles of claim construction applied to all other claim language, which are (1) that the language of the claim defines the scope of the protected inventions; and (2) that claims are to be construed in light of the specification. Bell Communications Research, Inc. v. Vitalink Communications

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[13] Although means-plus-function claims cover the corresponding structures disclosed in the specification and the equivalents thereof, "an accused device must also perform the identical function as specified in the claims." Valmont, 983 F.2d at 1042.

Corp., 55 F.3d 615, 619-20 (Fed. Cir. 1995). Furthermore, a question often arises as to whether or not language contained in a claim preamble should be deemed to be among the limitations of the claim. The Federal Circuit has held that "a claim preamble has the import that the claim as a whole suggests for it." Id. at 620. The Federal Circuit, revitalizing the holding of one of its predecessor courts, recently quoted Kropa v. Robie, 187 F.2d 150, 152 (C.C.P.A. 1951), as follows:

> [T]he preamble has been denied the effect of a limitation where ... the claim or [interference] count apart from the introductory clause completely defined the subject matter [of the invention], and the preamble merely stated a purpose or intended use of that subject matter. On the other hand, in those ... cases where the preamble to the claim or count was expressly or by necessary implication given the effect of a limitation, the introductory phrase was deemed essential to point out the invention defined by the claim or count. In the latter class of cases, the preamble was considered necessary to give life, meaning and vitality to the claims or counts.

Bell Communications, 55 F.3d at 620-21 (footnote omitted).

In this case, neither the word "controller" nor any similar word is found in the preamble or in any other portion of claim 1. The first reference to a "controller" in the patent specification occurs in the "Summary of the Invention," as follows:

> According to one aspect of the present invention, an array of Flash EEprom cells on a chip is organized into sectors such that all cells within each sector are erasable at once. A Flash EEprom memory system comprises one or more Flash EEprom chips under the control of a controller.

CX 1 at col. 1, lines 62-67 (emphasis added).

OUII argues that the highlighted sentence and several other portions of the specification define a "Flash EEprom system," as used in the preamble of claim 1, and further that an EEPROM memory chip is useless without a

controller or a microprocessor serving the same function as a controller. Respondents also argue that the specification requires a controller to be part of the claimed Flash EEprom system. However, while the specification assumes that a controller is necessary for the operation of the claimed EEprom system, claim 1 does not expressly claim a controller, and the above quoted language of the specification is ambiguous about whether the controller is part of the claimed Flash EEprom system.

It is first observed that "a Flash EEprom memory system" is not synonymous with the "EEprom system" claimed in the preamble of claim 1. Although the only linguistic difference between the two terms is the word "memory," it is evident from the contexts in which those terms are used in the `752 patent that they refer to different subject matter.

The "Flash EEprom memory system" described in the specification refers to an overall concept which is "one or more Flash EEprom chips under the control of a controller." This description is provided in the "Summary of the Invention" portion of the specification as part of an overview of the technology relevant to the patent. However, the "Flash EEprom system" of claim 1 is defined by the body of the claim.[14]

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[14] The relationship discussed above between the preamble of claim 1 and the specification of the `752 patent stands in contrast to circumstances such as those in Corning Glass Works v. Sumitomo Elec. U.S.A., Inc., 868 F.2d 1251, 1256-57 (Fed. Cir. 1989), relied on by OUII, in which the patentee took advantage of the specification to "set[] forth in detail the complex equation for the structural dimensions and refractive index differential necessary, in accordance with the invention, for an optical waveguide fiber comprising a fused silica core and cladding to transmit preselected modes of light," and then simply referred to "[a]n optical waveguide" in the preamble of the claim at issue.

Claim 1 covers a "Flash EEprom system" "comprising" each of the subsequent claim elements recited thereafter in the claim, but does not appear to include many items which would be included in the more general term in the Summary of the Invention.

In the case of claim 1 of the '752 patent, the preamble serves merely to state the intended purpose of the subject matter contained in the claim elements recited thereafter. In other words, the preamble tells the reader that claim elements recited after the preamble function together as an EEprom system. The preamble of claim 1 falls into the class of claims in which the preamble does not have the effect of a claim limitation.

Even if a "Flash EEprom memory system," as found in the Summary of the Invention, were synonymous with the "Flash EEprom system" of claim 1, it would not be apparent that a controller is necessarily part of the system. The referenced portion of the specification states that a Flash EEprom memory system "comprises one or more Flash EEprom chips under the control of a controller." Thus, a Flash EEprom memory system is one or more Flash EEprom chips. The phrase "under the control of a controller" provides additional information about the operation of the one or more Flash EEprom chips. The phrase need not be read in such a way as to make the controller part of the definition of the term Flash EEprom system in claim 1.[15] It appears merely to be descriptive, i.e., a statement that the chips operate under the control of a controller. Furthermore, other references to a controller in the specification strongly support the conclusion that a controller is part of the computer system in which the claimed invention operates although it is not part of the claimed invention itself.[16]

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[15] See also CX 1 at col. 5, lines 6-12 (discussed below in this section), in which the controller is referred to separately from the "Flash EEprom system."

[16] In their replies and proposed reply findings OUII and Respondents rely on the Abstract on the first page of the patent, which states in part that "[a] system of Flash EEprom memory chips with controlling circuits serves as non-volatile memory such as that provided by magnetic disk drives." The Abstract, which was supplied by the patentees as part of the application, is (continued...)

In the portion of the specification entitled "Description of the Preferred Embodiments," there is a subsection called "EEprom System" in which Figures of the patent specification are discussed. CX 1, col. 3, line 33 through col. 7, line 38. This description does not show the controller to be part of the claim. Rather, the specification teaches that a controller is used in connection with the preferred embodiments of the claimed invention. For example, according to the specification, a "computer system in which various aspects of the present invention are incorporated is illustrated generally in FIG. 1A." CX 1 at col. 3, lines 34-36. Thus, Fig. 1A contains a block representing a controller 31 as part of the computer system in which the present invention is incorporated in its preferred embodiment, yet the claims of the `752 patent are not drawn to a computer system and the specification does not state that the controller is part of the claimed invention.

The specification further explains that "[t]he bulk storage memory 29 is constructed of a memory controller 31, connected to the computer system bus 23, and an array 33 of EEprom integrated circuit chips." CX 1 at col. 3, lines 61-64. Similarly, in presenting the controller as part of the computer system, the specification also states that in "FIG. 1B, the controller 31 is preferably formed primarily on a single integrated circuit chip. It is connected to the system address and data bus 39, part of the system bus 33, as well as being connected to the system control lines 41, which include

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[16](...continued)
of necessity extremely abbreviated, and in this case vague as to the meaning of "controlling circuits." See CX 1; CX 6 (`752 Patent Prosecution History) at SD008704. The Abstract sheds no light on the question of whether a controller is a limitation contained in claim 1. Indeed, "[t]he purpose of the abstract is to enable the Patent and Trademark Office and the public generally to determine quickly from a cursory inspection the nature and gist of the technical disclosure. The abstract shall not be used for interpreting the scope of the claims." 37 C.F.R. § 1.73(b).

interrupt, read, write and other usual computer system control lines." CX 1 at col. 4, lines 3-8. See also CX 1 at col. 4, lines 27-36 (stating that for large amounts of memory, additional EEprom arrays can be connected to the serial data lines of the controller chip.) Figure 1B, like Fig. 1A, depicts the connection of the claimed invention to the computer system in the preferred embodiment. Thus, although the claimed invention is found within the parameters of the subject matter covered by the portions of the computer system depicted in Figs. 1A and 1B, those Figures and the corresponding textual discussion show that the controller is part of the computer system which is necessary to make the Flash EEprom system work, but is not part of the claim.

The arguments of OUII and respondents that a controller is necessary to make the Flash EEprom system work are unpersuasive. It is true that some form of outside control is necessary to make the Flash EEprom system work, but this does not make the controller part of the claim.

As discussed above, a controller is shown in the patent to address an array of flash memory chips and may be used with flash chips to mimic (or emulate) the operation of a disk drive.[17] See FF 43. Therefore, the patentees have shown that the claimed Flash EEprom system should be connected to a controller, and they provide a discussion of how the controller is to be used with their invention.

Fig. 2, like Figs. 1A and 1B also depicts a controller in connection with that Figure. The specification states that "A Flash EEprom system

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[17] The specification of the '752 patent discusses only a computer system with a hardware controller in connection with its preferred embodiments. However, if one chooses not to use a hardware controller, the function must be carried out by alternative means such as software that tells the host microprocessor how to address the flash memory chips. See FF 44; Mehrotra, Tr. 354-36; CX 1.

includes one or more Flash EEprom chips such as 201, 203, 205. They are in communication with a controller 31 through lines 209. Typically, the controller 31 is itself in communication with a microprocessor system (not shown)." CX 1 at col. 5, lines 6-12. In the first sentence of this quotation it is stated that the Flash EEprom chips are part of the Flash EEprom system. In the next sentence the patent teaches that the chips are connected to the controller. This discussion does not indicate that the controller is part of the claimed Flash EEprom system. This discussion is significant because the patentees expressly refer to their claimed "Flash EEprom system" separately from the controller, microprocessor and other devices which are contained in the entire computer system in which the claimed invention is employed.

Furthermore, the specification with respect to Fig. 2 teaches that a "Flash EEprom system" (which as required by the first element of claim 1 includes an array of Flash EEprom cells) is connected to the controller through lines 209 and therefore indirectly to the microprocessor. Thus, the patentees explain in the preferred embodiments how their claimed EEprom system is connected to the controller which in turn connects to a microprocessor.[18] In light of the discussion above, it would be erroneous to hold that the invention of claim 1 extends to the controller or any other device to which the Flash EEprom system is connected.

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[18] Again, the fact that a controller was thought by the patentees to be required in order for their invention to operate does not mean that a controller is part of the claimed invention. The operation of the claimed invention depends upon proper voltage, grounding, a microprocessor and many other variables and components originating or found outside the array of EEproms; yet it is not argued that they are covered by the claims of the '752 patent. See McGreivy, Tr. 1755-1756.

(b) **Means for Selecting**[19] ...

In addition to the preamble of claim 1, OUII argues that a controller also is required by the second recited element of claim 1, which is the "means for selecting a plurality of sectors among the one or more chips for erase operation."[20] Respondents also argue that if the construction of the "means of selecting" advanced by Complainant is accepted, then the "means for selecting" must include a controller, since the commands necessary to select blocks and erase them originate in the controller.

OUII argues that the "means for selecting" consists of all the circuitry and components described in CX 1, col. 5, lines 26-50, Figs. 3A and 3B. There is no dispute that the portion of the specification designated by OUII does in fact correspond to the "means for selecting."[21] Furthermore, as in the other portions of the specification, the patentees acknowledge and illustrate that the circuitry depicted in Figs. 3A and 3B depends upon the operation of other circuits within the computer system. However, a reading of the relevant portion of the specification and an examination of the referenced drawings does not support the conclusion that the recited claim element reads on a controller.

The portion of the specification that discloses a structure for the "means for selecting" element explains how a controller is used in the

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[19] The means for selecting is the second recited element in the '752 patent. The first recited element is not in dispute.

[20] A description of certain Flash EEPROM chips that are encompassed by the present invention is found in the patent specification at, for example, col. 4, line 66 through col. 5, line 24.

[21] Indeed, as discussed above in the section on the general law applicable to claim construction, because of the existence of means-plus-function elements in claim 1, reference must be made to the claim specification to understand the scope of the claim. Valmont, 983 F.2d at 1042.

relevant select and erase operations. For example, the specification states at col. 5, lines 26-42, as follows:

> FIG. 3A illustrates a block diagram circuit 220 on a Flash EEprom chip (such as the chip 210 of FIG. 2) with which one or more sectors such as 211, 213 are selected (or deselected) for erase. Essentially, each sector such as 211, 213 is selected or tagged by setting the state of an erase enable register such as 221, 223 associated with the respective sectors. The selection and subsequent erase operations are performed under the control of a controller 31 (see FIG. 2). The circuit 220 is in communication with the controller 31 through lines 209. Command information from the controller is captured in the circuit 220 by a command register 225 through a serial interface 227. It is then decoded by a command decoder 229 which outputs various control signals. Similarly, address information is captured by an address register 231 and is decoded by an address decoder 233.

As the above portion of the specification explains, circuit 220 depends upon receiving command information from the controller. It is not argued by Complainant nor would it be reasonable to assume that circuit 220 could operate in a vacuum. However, the means for selecting is not the command signal from the controller. Rather, it is circuit 220. It is plainly stated in the portion of the specification quoted above that it is "circuit 220 on a Flash EEprom chip (such as the chip 210 of FIG. 2) with which one or more sectors such as 211, 213 are selected (or deselected) for erase."

Circuit 220 is depicted in Figs. 3A and 3B. Figure 3B shows the structure of the register such as 221, 223 in more detail than Fig. 3A. Neither Figure depicts a controller, nor is a controller included within the circuit.[22]

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[22] As originally filed, the application for the '752 patent described Fig. 3A as "a block circuit diagram in the controller for implementing selective multiple sector erase according to the preferred embodiment," in the portion of the application entitled "Brief Description of the Drawings." CX 1 at SD008659. Subsequently, the applicants, through their agent, amended the application so as to change the phrase "in the controller" to "on a Flash EEprom chip," explaining that the reference to a controller in the original (continued...)

Most of the references to a controller that are relied on by the parties are contained in the portions of the specification entitled "Description of the Preferred Embodiments," under the subheadings "EEprom System" and "Erase of Memory Structures."

Additional discussions concerning a controller are found in the portions of the specification entitled "Defect Mapping" and "Write Cache System," which refer to Figures 5 through 8. It is evident that Figures 6 and 7 do not require a controller to be read into claim 1 and the claims at issue which depend therefrom.[23] An examination of the `752 patent's prosecution history shows that those Figures and the corresponding "Defect Mapping" portion of the specification were intended to support several claims that appeared in the patent application as originally filed, but which were subsequently canceled by the applicants as directed to a non-elected invention. See CX 6 at

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[22](...continued)
text was an inadvertent error, and that the "amended description is now consistent with the figures as well as the descriptions" in the relevant portion of the specification, which corresponds to col. 5, lines 26-28 of the `752 patent as issued. CX 6 at SD008659, SD008733, SD008736-008737; CX 1. The parties have placed little or no reliance on the prosecution history with respect to the issue of whether of not claim 1 covers a controller. The Administrative Law Judge finds that the prosecution history contains few references relating to whether a controller is part of the claims other than the discussion referenced in this footnote which provides some evidence that the controller is not part of the claims.

[23] The latter portions of the specification were not raised in the briefing until Respondents referred to Figs. 6 and 7 in their reply findings (in "see also" citations), and characterized these Figures as "depicting details of the controller circuitry as forming part of the read and write data path control." See RPRFF 30 and 32. Consequently, aside from the aforementioned arguments of Respondents, the parties have not addressed Figures 6 and 7 in their briefs. It is likely that had Respondents' arguments concerning Figs. 6 and 7 occurred in their main brief or initial proposed findings, Complainant would have provided its explanation for the Figures and the corresponding portion of the specification text. Indeed, Figures 6 and 7 do not appear to be crucial to any parties' arguments concerning the proper construction of the `752 patent claims.

SD008688-8693, SD008733, SD008736.[24]

Consequently, in view of the claim language, the specification text and drawings, as well as the prosecution history, the Administrative Law Judge determines that a controller is not included in the second claim element recited in the body of claim 1.

(b)(1) "a plurality of sectors"

Aside from the question of whether or not a controller is required by the second element recited in claim 1, there is also a dispute among the parties as to whether, as Complainant argues, the means for selecting covers a means capable of selecting simply a plurality of sectors (i.e., more than one sector) for simultaneous erase, or whether, as Respondents and OUII argue, the claimed invention is limited to a device capable of selecting any combination of sectors (i.e., any possible combination of sectors) for erase at the same time.

The claim language specifies only that the claimed invention contain a "means for selecting a plurality of sectors among the one or more chips for erase operation." There is nothing abstruse about the meaning of the phrase "a plurality." "A" refers or to an "undetermined, unidentified, or unspecified" noun. Webster's Third International Dictionary 1 (1976) ("Webster's"). The noun referred to in this case is "plurality." A "plurality" in its most common meaning is "the state of being plural," i.e., "relating to or consisting of or containing more than one ...." Id. at 1745. Therefore, according to the

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[24] The Administrative Law Judge recalls no testimony concerning the "Defect Mapping" portion of the specification during the hearing. Had it been known that Respondents' arguments would extend to Figs. 6 and 7, the Administrative Law Judge would have welcomed testimony concerning that portion of the specification, as well as relevant Patent and Trademark Office ("PTO") procedures concerning canceled claims and "non-elected" inventions.

plain language of the claim, the second recited element requires only that the means for selecting be capable of selecting more than one sector for erase; it does not require that the means be capable of selecting any combination of sectors whatsoever.

In addition to the plain language of the claim, the remainder of the specification must also be examined to see whether it provides guidance as to the meaning of the claim. As discussed above, all claims should be read in light of their specification. See, e.g., Markman, 52 F.3d at 979; Bell Communications, 55 F.3d at 619-20. With respect to means-plus-function claim elements, one "must construe the functional claim language `to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.'" Valmont, 983 F.2d at 1042 (quoting 35 U.S.C. 112, ¶ 6). Consequently, the means-plus-function elements of claim 1 of the `752 patent should be construed to cover the preferred embodiment disclosed in the specification.[25]

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[25] Complainant points out that in order to determine whether a means-plus-function claim is literally infringed, or "reads on," an accused device, one must determine whether the accused device performs the identical function specified in the claim, rather than comparing the accused device to the structure disclosed in the specification as required for other aspects of a means-plus-function claim. SanDisk's Post-Hearing Br. at 6-7 (citing Pennwalt Corp. v. Durand-Wayland, Inc., 833 F.2d 931, 934 (Fed. Cir. 1987), cert. denied, 485 US 961 (1988), and Valmont, 983 F.2d at 1042.)). However, that identity of function requirement does not conflict with or overrule the requirement discussed in connection with cases such as Markman, Bell Communications, and especially Valmont, to the effect that the functional claim language of a means-plus-function claim, like any other claim language, must be understood in the context of the entire specification.

Complainant also argues that "[w]here, as here, the meaning of the function disclosed in the element is unambiguously clear, the function may not be limited by the specification." SanDisk's Post-Hearing Br. at 7 (citing Envirotech Corp. v. Al George, Inc., 730 F.2d 753, 759 (Fed. Cir. 1984)). In Envirotech, the Federal Circuit stated that "what is patented must first be defined," and reiterated the well-established axiom of claim interpretation that "[w]ords in a claim `will be given their ordinary and accustomed meaning,

(continued...)

The preferred embodiment covers any combination of sectors for erase (unlike the plain language of the claim which refers only to "a plurality of sectors"). Thus the arguments of Respondents and OUII are that because the preferred embodiment shows the ability to select any combination, the claim must be so limited despite the claim language, "a plurality."

Nowhere in the specification of the '752 patent is the term "a plurality of sectors" expressly defined so as to be accorded anything other than its ordinary meaning. There are, however, various portions of the specification that one or more of the parties believes to be relevant to the issue of whether the claimed invention must be capable of selecting any combination of sectors for simultaneous erasure.

Early in the specification, the following is stated:

> The invention allows any combination of sectors to be selected and then erased simultaneously. This is faster and more efficient than prior art schemes where all the sectors must be erased every time or only one sector at a time can be erased. The invention further allows any combination of sectors selected for erase to be deselected and prevented from further erasing during the erase operation.

CX 1 at col. 1, line 67 through col. 2, line 6.

OUII and Respondents rely in part on this portion of the specification to support their argument that the claimed invention of claim 1 must have a means capable of selecting any combination of sectors for multiple erase. OUII Post-Hearing Br. at 9, 10; SPFF 89, 90; Respondents Post-Hearing Br. at

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[25](...continued)
unless it appears that the inventor used them differently.'" 30 F.2d at 759 (quoting Universal Oil Prods. Co. v. Globe Oil & Refining Co., 137 F.2d 3,6 (7th Cir. 1943), aff'd, 322 U.S. 471 (1944)). Complainants' argument is unpersuasive. This holding of the Federal Circuit is not a prohibition against examining the specification to determine whether the words in a claim should be given a specialized meaning. Indeed, one must refer to the specification to determine whether an applicant attributed any special meaning to the terms of a claim. Markman, 52 F.3d at 979-80.

47; RPFF 846, 847. As acknowledged by OUII and Respondents, this portion of the specification states certain "objectives" or "goals" of the claimed invention. However, "[r]eference to an object does not constitute in itself a limitation in the claims." Rolls-Royce Ltd. v. GTE Valeron Corp., 800 F.2d 1101, 1108 (Fed. Cir. 1986). Similarly, a mere "goal" stated in a specification does not cause a corresponding limitation to be read in to a claim. Intel Corp. v. U.S. Int'l Trade Comm'n, 946 F.2d 821, 836 (Fed. Cir. 1991)(where a "goal" of invention was to be capable of withstanding 300 hours of ultraviolet light exposure without erasing, accused device did not have to possess this capability in order to be infringing).

Similarly, in this case, although the portion of the specification quoted above "allows" (emphasis added) the selection of any combination of sectors for simultaneous erase, this text in the specification cannot be used to limit the plain language of claim 1. It does not act as a definition of any of the words or phrases used in claim 1, nor does it provide any explanation of an embodiment of the invention or how it functions.[26]

OUII and Respondents rely on other portions of the patent specification. In particular, they rely on the discussion and Figures depicting the preferred embodiment of the claimed invention, and the fact that the preferred embodiment is capable of selecting any combination of sectors for simultaneous

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[26] It is noted, especially in connection with the portion of the specification quoted above (col. 1, line 67 through col. 2, line 6), that the characterization of the invention of being able to select any combination of sectors for simultaneous erasure was made vis-a-vis the stated goal of faster and more efficient operation, in contrast to the prior art which required one to erase all sectors each time, or only one sector at a time. The goal of faster and more efficient operation is met by a device such as that employed by SanDisk in which one need not choose between selecting only one sector or all sectors for simultaneous erase, as in the prior art to the `752 patent. In other words the ability of a device to select almost any combination, or many combinations, for simultaneous erase meets the stated goal of the invention.

erase. They argue that the preferred embodiment is the only embodiment of the claimed invention contained in the `752 patent, and argue that since the second element is drafted in means-plus-function form, the claimed invention must be limited to a device capable of selecting any combination of sectors for erase.

Complainant argues that it is error to read the features of the preferred embodiment into the claims. SanDisk's Post-Hearing Br. at 6-7 (citing, inter alia, Laitram Corp. v. Cambridge Wire Cloth Co., 863 F.2d 855, 865 (Fed. Cir. 1988), cert. denied, 490 U.S. 1068 (1989)).

There is a general rule concerning the preferred embodiment of a specification, as held by the Federal Circuit, that "[r]eferences to a preferred embodiment, such as those often present in a specification, are not claim limitations." Laitram, 863 F.2d at 865 (citing SRI Int'l v. Matsushita Elec. Corp., 776 F.2d 1107 (Fed. Cir. 1985)(en banc)). Thus, the fact the preferred embodiment of the claimed invention of the `752 patent has a means for selecting any combination of sectors for simultaneous erase does not in and of itself mean that claim 1, and the second element in particular, must be construed to cover only devices capable of such an erase operation. This is particularly true where, as is the case here, the plain language of the claim is to the contrary.

However, OUII, relying on the recent Federal Circuit opinions in Ethicon Endo-Surgery, Inc. v U.S. Surgical Corp., 93 F.3d 1572 (Fed. Cir. 1996), and General American Transp. Corp. v. Cryo-Trans Inc., 93 F.3d 766 (Fed. Cir. 1996), and Respondents, relying on Ethicon, argue that in this case the preferred embodiment requires that one construe claim 1 to cover only means capable of selecting any combination of sectors.

In Ethicon, the claim at issue was for an improved lockout mechanism to

prevent the refiring of a surgical stapler. The claim provided that the lockout mechanism was to be located in the "staple cartridge." One of the questions to be determined was whether according to the claim the lockout could be located on the firing means of the device and still be considered to be within the "staple cartridge." The District Court relied on the patent specification, including a Figure depicting a "staple cartridge" in the preferred embodiment, to determine that the term "staple cartridge" should not be construed as broadly as plaintiff argued, and that the lockout could not be located on the firing means. On appeal, the plaintiff argued that the District Court had improperly read a particular embodiment from the specification into the claim. The Federal Circuit, in affirming the District Court on this issue, held that the District Court "did not import an additional limitation into the claim; instead, it looked to the specification to aid its interpretation of a term already in the claim, an entirely appropriate practice." 93 F.3d at 1578.

In this case, however, the term "a plurality" is not used in the specification in relation to the preferred embodiment. The specification states that "FIG. 3A illustrates a block diagram circuit 220 on a Flash EEprom chip ... with which one or more sectors ... are selected (or deselected) for erase." (emphasis added) The particular embodiment illustrated is capable of selecting any combination of sectors for erase. However, the specification in this instance does not provide a definition of any term or phrase in the patent claim. In fact the specification referring to "one or more sectors . . . selected (or deselected) for erase," appears to confirm the claim language "plurality" of sectors.

To determine that the second element of claim 1 claims only a device capable of selecting any combination of sectors would be to import a

particular element from the specification into the claim, not because the specification provides a definition for disputed claim language, but in order to narrow the claim based on the preferred embodiment. To refer to the specification to understand a term, as was done in Ethicon, is an appropriate way to read a claim in light of the specification. However, in this case, in view of the claim language "a plurality of sectors," to limit the claim because a certain feature is contained in the specification constitutes a classic error in claim construction.

In General American, the issue concerned the placement of openings in a refrigerated container (a railcar) through which carbon dioxide gas could escape, and the meaning of the term "adjacent," as used in the claim. The claim contained the limitation that there be a plurality of openings adjacent to "each of said side walls and said end walls" of the container. The accused railcar had openings adjacent to the side walls, but lacked openings adjacent to the end walls as required by the claims. The District Court used a dictionary definition of the term "adjacent" (i.e., "not far off" or "not necessarily at but nearby or near") to find that the endmost openings adjacent to the railcar's side walls also served as openings adjacent to the railcar's end walls. 93 F.3d at 769.

The Federal Circuit, in finding that the District Court erred in construing the claim, relied in part on the preferred embodiment of the specification to find that the claim required the opening to be adjacent to only one wall, the nearest one to which it directs the flow of carbon dioxide gas. The Federal Circuit noted that the preferred embodiment was in fact the only embodiment of the invention described in the specification. 93 F.3d at 770.

The relevant facts of the General American case are dissimilar to those

presented in this case. In General American, the patentholder and the District Court sought to expand the meaning of a term in a claim in contravention of the plain meaning imparted by the claim language, and by discounting the embodiment described in the specification. This case presents a contrary scenario in which Respondents and OUII seek to use the preferred embodiment described in the specification to limit the plain language of the patent claim.

Furthermore, it is not correct to read the Federal Circuit's opinion in General American to mean that if the preferred embodiment is the only embodiment described in a specification, then its conditions may serve as a limitation on the claim. Rather, the Federal Circuit's opinion stated that since there were no other descriptions of "adjacent" openings than that found in the preferred embodiment, there was a limited disclosure in the specification, which confirmed the plain language of the claim. Indeed, the Court continued by stating that "[n]othing in the claim language, specification, or drawings suggests" a contrary definition, and also stated that the prosecution history was "brief and not helpful to resolving the meaning of the disputed claim language." Id.

It is important to note that in General American, before turning to the specification to resolve the dispute concerning the meaning of the term "adjacent", the Federal Circuit first examined the claim language itself. In that instance there was a distinction made in the claim language between openings adjacent to the side walls and those adjacent to the end walls, precisely the distinction made by the specification. Id.

This case, in contrast, presents an instance in which the preferred embodiment is also the only embodiment found in the specification, yet the disputed feature found in that embodiment (i.e. the ability to select any

combination of sectors) is not similarly found as a limitation in the plain language of the claims. In this case, to require claim 1 to cover only devices capable of selecting any combination of sectors for erase would require the ordinary meaning of the terms of the second element of claim 1 to be forfeited in favor of a limitation found in the preferred embodiment. Clearly, such a limitation would involve an improper method of claim construction.

Respondents and OUII also state that claim 1 of the `752 patent as issued must be construed to cover only devices that are capable of selecting any combination of sectors for erase because of arguments that were made to the Examiner during prosecution. Their views are based on two statements made to the Examiner.

In construing a patent claim, one is required to consider the prosecution history if it is in evidence, as it is in this case. See Markman, 52 F.3d at 980. Indeed, the prosecution history "limits the interpretation of claim terms so as to exclude any interpretation that was disclaimed during prosecution."[27] Southwall, 54 F.3d at 1576.

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[27] In Standard Oil Co. v. American Cyanamid Co., 774 F.2d 448 (Fed. Cir. 1985), the Federal Circuit stated that:

> [T]he prosecution history (sometimes called "file wrapper and contents") of the patent consists of the entire record of proceedings in the Patent and Trademark Office. This includes all express representations made by or on behalf of the applicant to the examiner to induce a patent grant, or, as here, to reissue a patent. Such representations include amendments to the claims and arguments made to convince the examiner that the claimed invention meets the statutory requirements of novelty, utility, and nonobviousness. Thus, the prosecution history (or file wrapper) limits the interpretation of claims so as to exclude any interpretation that may have been disclaimed or disavowed during prosecution in order to obtain claim

(continued...)

As originally filed, Application No. 07/963,851, which led to the `752 patent, contained 62 claims. CX 6 at SD008655-008703. Most of the original claims (original claims 2, 3 and 10-62) were canceled at the outset of the prosecution as part of the Divisional Application Transmittal. CX 6 at SD008712. Of the original claims that remained (original claims 1, and 4-9), original claims 6 through 9 formed the basis of all final claims (i.e., claims 1-4) of the `752 patent as issued. CX 6 at SD008726, SD008737, SD008751. Eventually, all other claims remaining in the application were canceled at the applicants' request. CX 6 at SD008775.

In the Examiner's first Office Action, which was dated January 25, 1993, original claims 1, 4 and 5 were rejected. The Office Action also contained objections to original claims 6 through 9. The Examiner objected to claims 6 through 9 only because they were dependent upon original claim 1, which he

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[27](...continued)
allowance.

774 F.2d at 452 (emphasis added).

The interpretation of claims based on statements made during prosecution on behalf of the applicant is not to be confused with prosecution history estoppel. As the Federal Circuit explained in Southwall:

> Claim interpretation in view of the prosecution history is a preliminary step in determining literal infringement, while prosecution history estoppel applies as a limitation on the range of equivalents if, after the claims have been properly interpreted, no literal infringement has been found. The limit on the range of equivalents that may be accorded a claim due to prosecution history estoppel is simply irrelevant to the interpretation of those claims.

54 F.3d at 1578 (citation omitted).

As to whether the `752 patent covers only devices capable of selecting any combination of sectors for erase, the question of prosecution history estoppel need not be reached because the asserted claims are construed to read literally on devices capable of selecting "a plurality of sectors," and not necessarily any combination of sectors.

rejected under 35 U.S.C. § 102(a). However, he stated that if claims 6 though 9 were written in independent form, and included all of the limitations of the base claim (i.e., original claim 1) and any intervening claims, then original claims 6 through 9 would be allowable. CX 6 at SD008727.

In an Amendment dated May 24, 1993 and received by the PTO on May 27, 1993, the applicants, through their patent agent, added new claims 63 through 66, which were based on original claims 6 through 9 yet written so as not to depend from original claim 1. CX 6 at SD008733, SD008737-008738. Furthermore, in the Remarks made in connection with the May 27, 1993 Amendment and in other filings at the PTO, the applicants continued to seek allowance of original claims 1, 4, and 5, as well as original claims 6 through 9 (in their original dependent form) until, in an Amendment dated September 14, 1994 (received by the PTO on September 19, 1994) they canceled original claims 1, and 4 through 9. CX 6 at SD008761, SD008774-008776. Nevertheless, the prosecution history shows that added claims 63 through 66 issued as the claims of the `752 patent without any amendment and without any substantive remarks concerning those added claims. See SD008764, SD008775-008776, SD008777 (Notice of Allowability, dated Nov. 21, 1994).

Consequently, none of the statements now at issue were made to the Examiner with reference to the claims of the `752 patent. The statements at issue were made with reference to original claim 1 after the Examiner indicated that other claims (which form the basis for the claims at issue) would be allowed.

Nevertheless, remarks made to the Examiner concerning original claim 1 are potentially relevant to the construction of claim 1 of the `752 patent because claim 1 of the `752 patent is ultimately derived from a claim in the application that depended from original claim 1; and further, claim 1 of the

`752 patent is identical to original claim 1 (as initially filed before any amendment thereto), except for the final element recited in the body of claim 1 in the `752 patent which requires an "individual register." Thus, it is possible that during prosecution of the underlying application, the patent agent could have characterized some of the language in original claim 1 that might also apply to identical language in claim 1 of the `752 patent.

The first statement at issue was made by the patent agent in connection with the Amendment received on May 27, 1993. In that Amendment, applicants added claims 63 through 66, as discussed above, and, among other things, amended original claim 1 in an effort to obtain its allowance. Original claim 1 was amended to add the following limitation: "a bus for accessing said plurality of sectors." CX 6 at SD008733. Original claims 1, 4 and 5 had been rejected by the Examiner as anticipated by Sparks et. al. CX 6 at SD008727. Thus, in connection with the May 27, 1993 Amendment it was stated that "[c]laim 1 is being amended to more clearly distinguish over Sparks et al." CX 6 at SD008737. The Remarks continued by stating that claim 1 "recites a Flash EEPROM system having a plurality of erasable sectors addressable by a bus, and means for selecting and simultaneously erasing an arbitrary selection of sectors thereamong, the plurality of erasable sectors may be from one IC chip or pooled from several chips." CX 6 at SD008737.

Respondents and OUII argue that because the patent agent stated to the Examiner that original claim 1 had a means for selecting and simultaneously erasing an arbitrary selection of sectors, the "means for selecting" element of claim 1 of the `752 patent at issue in this investigation must be construed to require the selection of any combination of sectors.

However, it is not clear what the patent agent meant by the term "arbitrary" in the statement at issue. The word "arbitrary" ordinarily conveys

the concept of randomness or choice. See Webster's at 110. The patent agent did not provide any explanation of what he meant by "arbitrary" or "an arbitrary selection of sectors." So little was said by the patent agent concerning the supposedly "arbitrary" nature of the selections of sectors that it is doubtful at this time whether any weight should be accorded to his remarks. In this context, the use of the word "arbitrary" would not necessarily mean that there could be restrictions on the number of sectors that may be selected for simultaneous erase.

Furthermore, at issue is the patent agent's statement concerning an "arbitrary selection of sectors thereamong ...." "Thereamong" in the patent agent's statement refers to "a plurality of sectors addressable by a bus." A determination of exactly what the patent agent meant by the statement in question is complicated by the fact that original claim 1 was simultaneously amended to include the new recited element which limited original claim 1 to an invention with "a bus for accessing said plurality of sectors." It is not clear whether this new limitation played any role in the patent agent's decision to characterize the selection of sectors as "arbitrary" in the same sentence in which he also stated that the claimed Flash EEPROM system had "a plurality of sectors addressable by a bus." See CX 6 at SD008737.

Uncertainty as to what the patent agent was trying to convey is also recorded in the prosecution history. After the Amendment, the Examiner again rejected original claim 1, this time for indefiniteness. In fact, he found that the amendment had made the question of how the claimed invention operated "confusing," and asked: "Does the selecting means utilize the bus to select the plurality of sectors? Does the performing means use the bus or the selecting means to perform the erase operation?" CX 6 at SD008752.

Finally, the patent agent, on behalf on applicants, removed the

amendment from original claim 1, and eventually canceled the claim. CX 6 at SD008761, SD008776.

The effect of the amendment on original claim 1 with respect to the selecting means was confusing at the time it was made, and it remains confusing now. It is not clear whether the patent agent attempted to link the "arbitrary" nature of the selecting means to the indefinite amendment involving a bus to address the sectors, nor is it clear whether the word arbitrary was intended to convey an unlimited combination of sectors as disclosed in the preferred embodiment.

Therefore, for the reasons discussed above, the remarks made to the Examiner in connection with the May 27, 1993 Amendment concerning the "arbitrary" selection of sectors in amended original claim 1 were not clear with respect to original claim 1, and they do not now provide guidance concerning the correct construction of claim 1 of the `752 patent.

The other statement by the patent agent relied on by Respondents and OUII occurred in connection with an Amendment dated February 24, 1994, and received by the PTO on February 25, 1994. See CX 6 at SD008760-008763. In that Amendment, the applicants through their patent agent removed the new claim limitation discussed above concerning a bus, which was added in the May 27, 1993 Amendment. The patent agent also, inter alia, set forth additional arguments to differentiate the claimed invention of original claim 1 from the prior art, particularly the Sparks et al. reference.

The patent agent pointed out that Sparks et al. disclosed splitting the EEPROM array into two or more subarrays such that each subarray is configured and accessed as a separate memory chip. However, Sparks et al. was differentiated from the claimed invention of original claim 1 as follows:

Each time either a single chip can be selected for erase or all the

> chips can be selected for bulk erase. There is no provision as in Applicants' amended claim 1 for further partitioning each chip into flash sectors and allowing any combination of flash sectors within a chip or among all the chips of a memory system to be erased together. That is, Sparks et al. do not anticipate each chips "partitioned into a plurality of sectors, each sector addressable for erase such that all cells therein are erasable simultaneously; means for selecting a plurality of sectors among the one or more chips for erase operation; and means for simultaneously performing the erase operation on only the plurality of selected sectors."

CX 6 at SD008762.

Respondents and OUII rely on the fact that in this portion of the Remarks, the patent agent described the invention claimed in original claim 1 as "allowing any combination of flash sectors within a chip or among all the chips of a memory system to be erased together." The agent in the next sentence, however, referred to a "plurality of sectors."

As pointed out in Complainant's briefs, the patent agent did not need to go so far as to characterize the claimed invention of original claim 1 as being capable of erasing "any" combination of sectors together inasmuch as the Sparks prior art required one to choose between erasing only one chip or erasing all chips together. Therefore, a device capable of selecting a mere plurality of sectors for simultaneous erase would not read on the prior art.

On June 9, 1994, after the remarks quoted above were submitted to the Examiner, the patent agent had a personal interview with the Examiner. According to the Examiner's general description of the interview, "[t]he prior art was discussed and Mr. Yau [the patent agent] pointed out that none of the references disclosed a means for selecting a plurality of sectors among the IC chips." CX 6 at SD008771. Although this is not a detailed record of the interview, some weight should be given to the fact that the Examiner characterized the patent agent's arguments as going to the claimed invention's ability to select "a plurality" of sectors, and not "any combination" of

sectors as found once in the Remarks quoted above.

The patent agent's statements with respect to the term "any combination," and possibly the term "arbitrary," discussed above, were at worst imprecise. In this case the similarities and differences in meaning between "a plurality," "any combination" and an "arbitrary selection" take on special importance due to the devices at issue. Yet a device capable of selecting more than one sector but less than all sectors for simultaneous erasure would have avoided the prior art. A true understanding of the prosecution history is not to be gained by assessing the words exchanged between the patent agent and the Examiner against the context of the issues raised in this litigation, while ignoring the fact that the patent agent's statements (although they may have been imprecise or even erroneous given the hindsight provided by this case) did not affect the outcome of the patent prosecution with respect to the claims as they issued.

In Intervet America, Inc. v. Kee-Vet Laboratories, Inc., 887 F.2d 1050 (Fed. Cir. 1989), the Federal Circuit held, as follows:

> When it comes to the question of which should control, an erroneous remark by an attorney in the course of prosecution of an application or the claims of the patent as finally worded and issued by the Patent and Trademark Office as an official grant, we think the law allows for no choice. The claims themselves control.

887 F.2d at 1054.[28]

In declining to construe claims so as to contain limitations based on a patent attorney's erroneous remarks, the Federal Circuit in the Intervet case

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[28] A further application of the principle stated in Intervet is found, for example, in WHS Gaming, Inc. v. Int'l Game Technology, No. 94 C 3062, op. at 12 (N.D. Ill. Sept. 20, 1996), citing Intervet, in which the District Court stated that "[e]rroneous statements by a patent applicant or the applicant's attorney about what the claims cover cannot control over the clear language of the claims themselves."

observed that: "[t]he examiner was not mislead or deceived. The erroneous remark was not the end of the prosecution. The examiner was fully aware of what claims he was allowing." Id.

Similarly, in this case the claim language calls merely for a means to select "a plurality" of sectors for erase. The claim language was not changed to require "any combination" of sectors or any similar limitation. Furthermore, the Examiner's subsequent notes, discussed above, support the conclusion that the patent agent's remarks did not have an unintended (or intended) effect of leading the Examiner to an incorrect assumption about the scope of the claimed invention. In fact, as detailed earlier in this discussion, the Examiner indicated that he would allow claims like those asserted in this investigation before the Remarks at issue were made.

In addition, an important reason for not reading an "any combination" limitation into claim 1 of the `752 patent based on the Remarks quoted above is that the invention described in those Remarks is not the same invention claimed in the present claim 1 as issued.

Claim 1 of the `752 patent contains a limitation found initially in original claim 6, i.e., the fourth and last element recited in claim 1, an "individual register associated with each sector for holding a status to indicate whether the sector is selected or not." At the time that the Examiner indicated the allowability of original claim 6, that limitation was the only difference between dependent, original claim 6 and independent, claim 1 as originally filed. CX 6 at SD008687-008688, SD008761. Since the only difference between original claim 1 and claim 1 as issued is the "individual register" element contained in original dependent claim 6, this latter element must be construed in order to determine how the selection of sectors takes

place.[29]

(c) "Means for Simultaneously Performing the Erase Operation on Only the Plurality of Sectors

The third recited element in the body of claim 1 is a "means for simultaneously performing the erase operation on only the plurality of selected sectors." CX 1.

The structures which correspond to the erase means claimed in this element of claim 1 are the registers and the associated erase enable command. The erase of a sector is conditional upon the status that is stored in its associated individual register. See Guterman, Tr. 563-564; Harari, Tr. 232. The structures corresponding to this claim element are found in Figs. 3A and 4 (item 5), and the portions of the specification that describe those Figures. See, e.g., CX 1 at col. 6, lines 3-29; Mehrotra, Tr. 379-380.[30]

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[29] [[C]]
Although it is found that as a matter of claim construction, claim 1 of the `752 patent is not limited to devices capable of selecting any combination of sectors, but to a plurality of sectors, a determination of whether the particular design used by SanDisk is covered by the `752 patent is discussed below in the section of this Initial Determination on the domestic industry.

[30] The above interpretation is similar to the argument of OUII that "the specification discloses that the structure satisfying the `means for simultaneously performing' the erasure element includes components that are also required to satisfy the `means for selecting' element, along with additional circuitry to generate and distribute the global erase command." OUII Br. at 9-10; SPFF 82-89.

Respondents do not argue that there are other portions of the specification that correspond to the third recited element. However, they argue that the patent specification does not satisfy the requirements of 35 U.S.C. § 112 because it does not show how the outputs of the erase enable registers and the AND gate (both depicted in Fig. 3A) connect to the memory cells of the array. Furthermore, they argue that the specification does not disclose a charge pump which is alleged to be the best mode known to the inventors of combining the

(continued...)

(d) "Individual Register ..."

The fourth, and final element recited in the body of independent claim 1 of the `752 patent is an "individual register associated with each sector for holding a status to indicate whether the sector is selected or not." CX 1.

In accordance with their argument that the invention claimed by the `752 patent must be capable of selecting any combination of sectors for simultaneous erase, Respondents and OUII argue that the term "individual" as used in claim 1 requires a one-to-one correspondence between registers and sectors such that each sector has a register dedicated exclusively and entirely for its own use. In that way, the status of each sector is independent of the status of all other sectors because each sector's register operates exclusively for that sector.

Complainant argues that an individual register may consist of more than one latch,[31] and that a unique combination of latches may serve as an "independent register." By this definition of "individual register," one of the latches that works in a unique combination to form the register for any particular sector may also function in other combinations which are associated with other sectors.[32]

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[30](...continued)
erase voltage and the outputs of the selected registers for applying the erase voltage to the sectors. See Respondents' Br. at 35-40. However, as addressed below in the section concerning patent validity, the asserted claims of the `752 patent satisfy the enablement and best mode requirements.

[31] A "latch" is a logic element that temporarily stores one bit of information. Harari, Tr. 65. The word "latch" is commonly used to refer to a one bit switch. Frey (Tutorial) Tr. 104; Allen, Tr. 1031.

[32] The significance of this dispute among the parties in this investigation is that if the construction proposed by Respondents and OUII were adopted in this Initial Determination, Complainant SanDisk's devices could not be found to practice (or "infringe") claim 1 of the `752 patent, at least not literally. As discussed in the section concerning the domestic
(continued...)

The specification does not provide a definition of the term "individual" or "individual register." Thus, the words must be given their ordinary meaning. See Markman, 52 F.3d at 980 ("[A]ny special definition given to a word must be clearly defined in the specification."); Intellicall, Inc. v. Phonometrics, Inc., 952 F.2d 1384, 1387 (Fed. Cir. 1992)(words in a patent should be given their ordinary meaning to one of ordinary skill in the art if it does not appear from the patent or the file history that the terms were used differently by the inventors).[33]

The most common meaning for the adjective "individual" is "of, belonging to, arising from, or possessed by, or used by an individual." Synonyms for the adjective "individual" are "characteristic" and "special." Webster's at 1152. Something may, for instance, be "of," or be "used by" a person or thing yet still belong to or be used by someone or something else. Similarly, something may be "characteristic" of a person or thing yet not be exclusively the domain of any one person or thing.

In this case, the word "individual" does not indicate that the latches of a register cannot at least in part be used by more than one sector. A unique combination of latches may be said to be "characteristic" of a particular sector and to "belong to" it, without further implying that each of the latches involved is dedicated solely for the use of that sector.

The evidence adduced in this investigation shows that in the relevant art it is not uncommon for a register to be made up of more than one latch.

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[32](...continued)
industry, SanDisk's devices contain this claim element.

[33] The prosecution history does not provide additional evidence concerning the fourth and final element of claim 1. As discussed in detail, supra, this element and original claim 6 were accepted by the Examiner at the commencement of the prosecution on the basis of the application which became the specification, without further Amendment or Remarks by the patent agent.

The term "register" is well understood in the semiconductor industry to mean circuitry that stores information, typically on a temporary basis. Harari, Tr. 61; Guterman, Tr. 448. It is common for a register to be implemented by setting more than one latch to store the information. Harari, Tr. 61-63; Mehrotra, Tr. 316; Guterman, Tr. 448, 552-553; CX 198.

Unlike the second and third elements recited in the body of claim 1 of the `752 patent, this fourth element is not written in means-plus-function form. Thus, although it must be read in light of the specification as in the case of any claim element, it does not depend on the structures disclosed therein to the extent that a means-plus-function element would.

In the specification of the `752 patent, only the preferred embodiment is disclosed. The preferred embodiment is structured in such as way as to give the maximum amount of flexibility in the selection (or deselection) of sectors for erase, by depicting a device in which each sector has a register dedicated exclusively for its use. The registers shown are composed of one latch. However, there is no indication in the claim language or specification that the claimed invention is restricted to the preferred method of constructing registers and arranging them in an exclusive, one-to-one correspondence with the sectors. To construe claim 1 of the `752 patent to cover only such a structure would be impermissibly to read a limitation into the claim based upon the specification. See Laitram, 863 F.2d at 865 (citing SRI Int'l v. Matsushita Elec. Corp., 776 F.2d 1107 (Fed. Cir. 1985)).

2. Claim 2

Claim 2 of the `752 patent is as follows:

> The Flash EEprom system according to claim 1, wherein the simultaneously erasing means is responsive to the status in each of the individual registers, such that

only the selected registers are included in the erasing.

CX 1 at col. 17, lines 4-7.

The `752 patent discloses an EEPROM array in which the simultaneously erasing means is responsive to the status in each of the individual registers such that only the selected sectors are erased. The preferred embodiment is illustrated in Fig. 3A of the `752 patent. However, there is nothing in the claim language or the specification to require that the claimed invention be limited to the preferred embodiment. See Allen, Tr. at 1100-1101; RPX 31(E); Complainant's Reply FF at 87. This claim depends from claim 1 and requires that the means for performing the simultaneous erase be responsive to the status of the registers that correspond to the selected sectors in combination with the erase voltage. See RX 211 (Harari Dep.) at 68-69; Complainants' Resp. to Samsung PFF at 85.

3. Claim 4

Claim 4 of the `752 patent is as follows:

> The Flash EEprom system according to claim 1, wherein all the individual registers are simultaneously resettable to a status indicating the associated sectors as not selected.

CX 1 at col. 8, lines 4-7.

Claim 4 depends from claim 1 and requires the capability to erase all the sectors at once. This is accomplished by having individual registers that are simultaneously resettable to a status indicating that the associated sectors are not selected. The `752 patent discloses the preferred embodiment of the invention of claim 4 in Figure 3A. In the preferred embodiment, a reset signal is provided simultaneously and globally to all of the erase enable registers, resetting each register to "0," which is the nonselected

status. See Allen, Tr. 1102; Complainant's Reply FF 87-88. However, there is nothing in claim 4 of the specification to indicate that the claimed invention is limited to the use of a reset signal in the exact manner disclosed in connection with the preferred embodiment of the specification.

C. **Claim 27 of the `338 Patent**

Claim 27 of the `338 patent is as follows:

> In an array of addressable semiconductor electrically erasable and programmable memory (EEprom) cells on an integrated circuit chip, the memory cell being of the type having a source, a drain, a control gate and an erase electrode receptive to specific voltage conditions for reading, programming and erasing of data in the cell, and having a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell, such that a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions, a system for programming data to EEprom cells including means for temporarily storing a chunk of data for programming a plurality of addressed cells, means for programming in parallel the stored chunk of data into the plurality of addressed cells, and means for verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data, wherein the improvement comprises:
>
> means for inhibiting further programming of correctly verified cells among the plurality of addressed cells; and
>
> means for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly.

CX 2 at col. 26, lines 28-54.

Portions of the claim's lengthy preamble and the additional claim elements are at issue. According to Complainant a key feature of the claim 27 invention is allowing the programming of a chunk of cells in parallel, but treating each cell as if it were programmed individually for purposes of verification and inhibiting further programming of verified cells. Harari, Tr. 261-264 The preferred embodiment of claim 27 of the `338 patent describes a multi-state rather than a binary semiconductor device. The claim, however is not limited to the multi-state device. See e.g., CX 2 at col. 11, lines 56-61. Each of the portions of claim 27 which are in controversy will be

discussed below.

1. The Erase Electrode Element

The preamble of claim 27 recites as one of its elements "an erase electrode receptive to specific voltage conditions for reading, programming and erasing of data in the cell."

The term "erase electrode" is found in the `338 patent only in the claims.[34] CX 2. The term "electrode" is commonly understood in the semiconductor industry as a terminal to which an electrical signal is applied to perform some function. Pathak, Tr. 792, 918. An "erase electrode" is understood in the semiconductor industry as a terminal to which erase voltage conditions are applied to draw electrons off the floating gate. Pathak, Tr. 792. Thus, because the term "erase electrode" is not defined in the `338 patent as having anything other than its ordinary meaning, it is properly construed in the context of claim 27 as any terminal in a flash memory device to which erase voltage conditions are applied to draw electrons off the floating gate.

Respondents do not expressly contest this definition of "erase electrode" but argue that as used in the `338 patent, the term requires a separate structure for each cell which is dedicated specifically to drawing electrons off the floating gate. See, e.g., Respondents' Post-Hearing Br. at 20-21. Neither Complainant nor OUII adequately support this argument concerning the erase electrode.

Although the erase gate is used in the preferred embodiment as an erase electrode, various structures or terminals in a flash memory device can also

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[34] See CPFF 257; SPFF 98.

function as an erase electrode as that term would be commonly understood, including the silicon substrate. Harari, Tr. 77-83. Indeed, the record shows that various companies (which are not parties to this investigation) have used the substrate instead of an erase gate as the terminal to which erase voltage conditions are applied to draw electrons off the floating gate during the erase operation. Harari, Tr. 77-83; CPX 25.

Respondents further argue that the silicon substrate cannot serve as an erase electrode in its devices because claim 27 requires that the erase electrode be "receptive to specific voltage conditions for reading, programming and erasing of data in the cell," and that [

[C]

] Respondents' Post-Hearing Br. at 21. As addressed below in the section on the infringement issue, it is found that at least certain of respondents devices satisfy this claim element.

2. The Increment/Decrement Element

The preamble of claim 27 imposes the limitation that the memory cell have "a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell, such that a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions."

All of the devices at issue in this investigation (Samsung and SanDisk devices) are binary devices.[35] Complainant argues that for a binary device,

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[35] As discussed in the Background section of this Initial Determination, "multi-state" -- or "multi-level" -- devices are not currently in commercial use. See FF 30.

this element of claim 27 should be interpreted to cover a cell that achieves the programmed state by increment of the charge level with successive applications of programming voltage conditions, or a cell that achieves the erased state by decrement of the charge level with successive applications of erasing voltage conditions (or a cell that can perform both of these functions).

Respondents argue that the portion of claim 27 at issue includes two limitations: one requiring the successive application of voltage conditions to program (by putting charge on the floating gate) and the other requiring the successive application of voltage conditions to erase (by removing charge from the floating gate). They argue that "without the term 'or' this claim would merely recite counteracting applications of programming and erasing voltage conditions repetitively incrementing and decrementing charge without any net change in the charge level on the floating gate." Respondents' Post-Hearing Br. at 20-21.

OUII takes the position that claim 27 does not require successive applications of both programming voltage conditions and erasing voltage conditions.

Respondents argue that Complainant's interpretation of the word "or" allows for a broader construction of the patent claim than their interpretation. Citing the Federal Circuit's opinion in Athletic Alternatives, Inc. v. Prince Mfg., Inc., 73 F.3d 1573, 1581 (Fed. Cir. 1996), they argue that a court should adopt the narrower of two possible constructions, and that this element of claim 27 should be construed to cover only a device that achieves a specific memory state through successive applications of voltage, during programming and erasing. Respondents' Reply Br. at 10.

In Athletic Alternatives, the Federal Circuit highlighted the fact that patent claims perform the function of putting others on notice of the boundaries of the invention, and held, as follows:

> Where there is an equal choice between a broader and a narrower meaning of a claim, and there is an enabling disclosure that indicates that the applicant is at least entitled to a claim having the narrower meaning, we consider the notice function of the claim to be best served by adopting the narrower meaning.

Id. at 1581.

However, claim 27 of the `338 patent does not present a case of an equal choice between two meanings. The simplest meaning of the claim element at issue is that one may use successive applications of programming voltage conditions or successive applications of erasing voltage conditions in order to practice the claimed invention. The word "or" in this instance serves its normal function of indicating the availability of an alternative or a choice. Webster's at 1585.

Respondents would read an additional limitation into the claim by requiring that in every instance in which one sought to change the charge level of a cell one must make successive applications of programming or erasing voltage conditions. That additional limitation is not required by the language of the claim. Consequently, based on the plain language of the claim, there is not an equal choice to be made.

Furthermore, other evidence found in the specification and adduced at the hearing supports the broader construction of the claim. The increment/decrement element at issue corresponds to the programming algorithm illustrated in Fig. 15 (item 6), which is described in the text at col. 19, line 57 through col. 20, line 16, whereas the erasing algorithm is illustrated separately in Fig. 11 (items 1 and 2), which is described at col. 16, lines

18-25. With respect to both of these algorithms the charge on the floating gate is changed incrementally.

Thus, in the preferred embodiment disclosed in the specification, the patentees provided examples of incremental programming and of incremental erasing. See CX 2 at col. 18, lines 21-29. However, the fact that the preferred embodiment provides an example of each incremental operation does not mean that an additional limitation should be read into claim 27 that requires both incremental operations in all operations covered by the claim. See Loctite Corp. v. Ultraseal Ltd., 781 F.2d 861, 867 (Fed. Cir. 1985) ("Generally, particular limitations or embodiments appearing in the specification will not be read into the claims."); see also E.I. DuPont de Nemours & Co. v. Phillips Petroleum Co., 849 F.2d 1430, 1433 (Fed. Cir.), cert. denied, 488 U.S. 986 (1988) (prohibiting the reading of limitations from the specification into the claims "wholly apart from any need to interpret what the patentee meant by particular words or phrases in the claim").

The application of voltage conditions for programing and the application of voltage conditions for erasing are independent of each other, Harari, Tr. 1861, 1870. In both binary and multi-state devices, one may design for incremental programming and/or incremental erasing. However, programming and erasing are not part of the same operation. Harari, Tr. 1869; Pathak, Tr. 937.

Furthermore, in a multi-state device the reason for using incremental erasing is different from the reason for using incremental programming. In a multi-state device, different charge levels should correspond to different data. However, the consequences of over-erasing are endurance-related. The effect of over-erasing is not catastrophic to the performance of the device. Harari, Tr. 1870; Tutorial (Harari) Tr. 75-77; Guterman, Tr. 577-578.

Consequently, given the technical context in which the wording of claim 27 arose, it is proper that the claim be accorded the more ordinary, less complex meaning, such that one may use successive applications of either programming or erasing voltage conditions. It is not required that one use both program and erase incrementally in order to practice the claimed element.

3. The Temporary Storage Means

The preamble of claim 27 recites as one of its elements a "means for temporarily storing a chunk of data for programming a plurality of addressed cells." Complainant argues that in the context of this claim, the term "temporarily storing" would be understood by one of ordinary skill and should be interpreted to mean that the data for each cell is stored impermanently, but at least long enough to complete the programming of that cell. OUII argues that "temporarily storing" should be construed to mean storing as long as the individual cell in the chunk continues to receive the programming conditions. However, Respondents argue that "the term `temporarily' must be construed to mean during the entire programming process for the entire chunk of data and not merely until a cell has been verified once." Respondents' Post-Hearing Br. at 22.

The evidence of record shows that in the context of the `338 patent, the term "temporarily storing" would be understood by one of ordinary skill to refer to a period of storage lasting at least as long as but not necessarily longer than the amount of time necessary to verify and terminate programming to the cell to which the stored data relates. After the programming of a cell is completed, the information used to program that cell is not used again. Harari, Tr. 248-249.

In claim 27 the patentees could have simply called for a means of

storing a chunk of data for programming.[36] However, they elected to add the word "temporarily" to the claim language. The term "temporarily" ordinarily means "for a brief period: during a limited time: briefly." Webster's at 2353. Thus, by adding the word "temporarily" the patentees have emphasized the brief nature of the data storage. That tends to support the claim interpretations proposed by Complainant and OUII, rather than Respondents. The brief nature of data storage is confirmed by reference to the specification and other evidence.

The means in question is disclosed in Figure 5, including block 190 (labeled "Read/Program Latches and Shift Registers"). Harari, Tr. 247-249; Thomas, Tr. 1509-1511; CX 2, at col. 19, line 27 through col. 20, line 36. It may be that in the preferred embodiment the data is stored in the latches until verification has occurred for the entire chunk of data stored therein, yet there is no express requirement to that effect. Thomas, Tr. 1510-1511; Pathak, Tr. 939. Moreover, after a particular cell to be programmed is verified, the data stored in the latch 190 serves no function for the cell that is already programmed, while the programming continues for the rest of the chunk. Harari, Tr. 247-249; Mehrotra, Tr. 329; Guterman, Tr. 587-588.

One of ordinary skill in the art knows that once programming and verification has taken place, the job is done for the stored data, and that "temporarily" in that case would mean just until the job is done. Pathak, Tr. 940-944. Thus, this element of claim 27 should not be construed so as to require storage of all data in a chunk until all cells to be programmed in accordance with the chunk of data have been programmed and verified. The data

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[36] In the context of the '338 patent a "chunk" is "typically several bytes," and may be used to refer to the number of cells required to program the chunk. CX 2 at col. 19, lines 10-12.

need be stored only long enough for the programing and verification of the particular cell.

4. The Parallel Programming Means

The preamble of claim 27 of the `338 patent recites as one of its elements a "means for programming in parallel the stored chunk of data into the plurality of addressed cells." Complainant argues that in the context of claim 27, the phrase "programming in parallel" should be construed as referring to the function of simultaneously programming a plurality of cells, without reference to the manner of programming used. Respondents argue that the parallel programming means is limited to devices that program using a Hot Electron Injection ("HEI") programming process.[37] See Respondents' Post-Hearing Br. at 24.

Figure 14 of the `338 patent discloses certain structures with which the parallel programming function can be performed. CX 2 at col. 5, lines 40-41, col. 19, lines 27-41; Mehrotra, Tr. 330. In particular, Figure 14 shows an embodiment in which a Program Circuit with Inhibit, block 210, performs the parallel programming function, with the source multiplexer (or "mux") 107 and the drain mux 109 providing the data path. CX 2 at col. 19, lines 27-41; Mehrotra, Tr. 330-334. Thus, the parallel programming means should be construed to include these structures or their equivalents.

The cells in the preferred embodiment of the `338 patent are connected in a NOR architecture configuration. Pathak, Tr. 812-813. HEI programming is thus appropriate for use with the cells described in the preferred embodiment. Harari (Tutorial), Tr. 51-52; Mehrotra, Tr. 334-335. However, the language of claim 27 is silent on the cell structure and the corresponding programming

[37] HEI as well as the Fowler-Nordheim method of programming are discussed in the Technological Background section. See FF I 17-22.

method that must be used. Indeed, the `338 patent is not a patent on cell architecture such as NOR or NAND, and which programming method should be used with a particular cell structure. The patent merely recites the broad, general function of "programming in parallel" without specifying the programming method. One of ordinary skill in the art would know that parallel programming can be achieved in more than one way depending on the type of cell structure selected in a device. Furthermore, circuit designers are familiar with the various methods of programming cells depending upon their structures. Pathak, Tr. 944-946; Harari, Tr. 1861-1865. Thus, claim 27 should not be construed to require HEI programming.

In claim 27 of the `338 patent, "programming in parallel" means that programming takes place for more than one cell at a time, such that all cells selected for programming in accordance with a chunk of data receive programming conditions at the same time. See Harari, Tr. 76; Pathak, Tr. 807-808; CX 2 at col 19, lines 30-31 ("The EEprom array 60 is addressed by N cells at a time.").

5. The Verifying Means

The preamble of claim 27 recites as one of its elements "means for verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data."

The record evidence shows that the term "verifying" as it is used in claim 27 of the `338 patent normally would be understood by one of ordinary skill to refer to the process of determining whether the data in a memory cell matches the data that is targeted to be written into the cell.[38] Guterman,

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[38] Mr. Thomas, Respondents' expert on whether Complainant SanDisk practices the `338 patent and on whether Samsung infringes the `338 patent, testified that the term "verify" is ordinarily used very loosely in the (continued...)

Tr. 489-490, 499. The `338 patent contains no contrary or inconsistent definition of the term.

However, Respondents point out that the claim language requires that the programmed data be verified "with" the chunk of stored data, and argue that claim 27 must read only on a device that verifies through the use of a comparator, as in the only structure disclosed in the `338 patent specification for verifying.

Questions are therefore raised as to whether claim 27 should be construed to require the use of a comparator, and whether a structure designed for use in a binary device can be equivalent to the structure disclosed in the `338 patent. These are especially pertinent questions because the Samsung and SanDisk devices at issue are binary devices and [[C]]

In a multi-state device, such as that described in the `338 patent's specification, a cell can be in one of several states. In performing the verification function, the first step is to determine the state of the cell to be verified (e.g., 0, 1, 2, 3). After determining the state the cell is in, the next step is to determine whether the cell is in the target state for that cell. If the cell is in the target state, the cell is verified; if not, further programming is required. Guterman, Tr. 490-493; CPX 46.

In a binary device, before programming can begin all cells must be in the erased state. Guterman, Tr, 493-495; CPX 48. Inasmuch as all cells start in the erased state, if the targeted state of a particular cell is the erased state, then the cell is in the targeted state before the programming cycle

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[38](...continued)
semiconductor industry to refer to the process of determining whether a cell is finished programming. Thomas, Tr. 1594-1595.

begins, and therefore no further action needs to be taken with respect to that cell. Harari, Tr. 264-265; Guterman, Tr. 493-495, 499-503; CPX 48. If the targeted state of a particular cell is the programmed state, and if the cell is not in the targeted state before the programming cycle begins, then programming pulses must be applied to bring the cell to its targeted state. Guterman, Tr. 493-495; CPX 48. For cells targeted to be in the programmed state, the cell is read after each programming pulse to verify whether the cell is in the programmed state (i.e., reads a "1"). Once the cell is sensed to be in the programmed state, further programming to that cell is terminated. Guterman, Tr. 493-495; CPX 48.

Figure 11-E of the `344 patent (which is incorporated by reference into the `338 patent) discloses circuitry that corresponds to the verify means in a multi-state implementation of the claim 27 invention. Figure 11-E depicts a multi-state implementation for a single cell in which the cell is able to hold one of four states. CX 2 at col. 4, lines 23-30; Guterman, Tr. 498-499; CX 3 (the `344 Patent); CPX 64. Figure 11-E discloses four sense amplifiers, one associated with each of the four states that the cell can hold., Each of the four sense amplifiers senses whether the current passing through the cell is greater or lesser than the reference current corresponding to the state associated with that sense amplifier. In the multi-state embodiment disclosed in Figure 11-E, once the sense amplifiers perform their sensing operation, the results are fed into the comparator disclosed in Figure 11-E, which determines whether the state of the cell matches the targeted state of the cell. Guterman, Tr. 499-503; CX 3, Fig. 11-E.

A binary embodiment equivalent to that disclosed in Figure 11-E of the `344 patent would not require all the circuitry disclosed for a multi-state implementation. Guterman, Tr. 499-503. In a binary device, it is unnecessary

to have more than one sense amplifier to perform the verification function of claim 27, since the only decision or verification that the device has to make is whether the cell is in the programmed state. Guterman, Tr. 499-503; Allen, Tr. 1173; CPX 64, CPX 66. For a binary device, it would be logical for a circuit designer to simplify the structure of Figure 11-E by eliminating three of the four sense amplifiers and the buffers and circuitry uniquely associated with those sense amplifiers, since they serve no function in a binary device and unnecessarily occupy surface area on the chip.[39] Furthermore, with a single sense amplifier, it is unnecessary to have a separate comparator circuit, since that comparator would merely replicate the function of the sense amplifier.[40] Guterman, Tr. 499-503; CPX 64, 66.

Consequently, the structure disclosed in Figure 11-E of the `344 patent could be reduced to a circuit with a single sense amplifier and no comparator for use in a binary device, and such a structure would be the structural equivalent of Figure 11-E. It could also be used to perform the function of verifying that addressed cells are in the correct state.

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[39] Dr. Allen, Respondents' expert on the issue of patent validity, testified that a device that only verifies whether the cell is in the programmed state would satisfy the verify means of claim 27. As discussed further below in the section on patent validity, Dr. Allen testified that the "means for verifying" element of claim 27 is satisfied by the M293, a binary device that, like the SanDisk and Samsung flash memory devices, performs the verification function using a single sense amplifier (without a separate comparator circuit) to ascertain whether cells targeted to be programmed have reached the programmed state, while ignoring the cells targeted to remain in the erased state. See Allen, Tr. 1178-1180.

[40] The `344 patent expressly discloses that a single sense amplifier and a single reference level can be used to differentiate between conduction states "1" (which could indicated "programmed") and "0" (for "erased"). CX 3 at col. 26, lines 55-60. In fact, the `344 patent teaches that in a four-state storage device the comparison may be accomplished with four consecutive read cycles and only one sense amplifier, with a different reference applied at each cycle, if the additional time required for reading is not a concern. CX 3 at col. 25, line 64 through col. 26, line 17.

Figure 16 of the `338 patent discloses certain additional structures for performing the verification function in a multi-state device. In the circuit compare module 703 shown in the Figure, the read bits are compared bit by bit with corresponding program data bits, i.e., it is determined whether there is a match between the read and write data.[41] This is performed by XOR (exclusive OR) gates such as 711, 713 and 715 shown in Fig. 16. The specification states that the number of such XOR gates used depends upon the number of binary bits encoded for each cell. The output of the XOR gates passes through a NOR gate 717 whenever all the bits are verified, and node 726 is taken high so that latch 721 is set in the verified state. Once latch 721 is set, the cell is inhibited from further programming during subsequent programming pulses that may be applied on the chunk. If, however, the read data does not match the write data, then latch 721 remains in its previous state.[42] Mehrotra, Tr. 339-340; CX 2 at col. 20, lines 17-51.

The Figure 16 multi-state embodiment could be modified for a binary device by making some simplifications to the structures that would be obvious to an ordinary flash memory circuit designer. Mehrotra, Tr. 342; Pathak, Tr. 819-820.

In fact, the `338 patent contemplates an embodiment with only two states. The `338 patent expressly states in the context of discussing the verification function that "if each memory cell is to store K states, then at

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[41] In the preferred embodiment, "[C]ircuit 200 comprises N cell compare modules such as 701, 703, one for each of the N cells in the chunk." CX 2 at col 20, lines 18-20.

[42] Figure 5 also provides a general identification of a "Compare Circuit", block 200, that performs the verify function in one embodiment of claim 27. The Program Circuit with Inhibit disclosed in block 210 of Figure 5 of the `338 Patent performs the function of inhibiting further programming by removing high voltage from the drain of the cell to be inhibited. Guterman, Tr. 508-510; Harari, Tr. 258, 267-269.

least K - 1, or preferably K reference levels need be provided. In one embodiment, the addressed cell is compared to the K reference cells using k sense amplifiers in parallel. This is preferable for the 2-state case because of speed ...." CX 2 at col. 11, lines 56-61. In other words, in the case of a two-state device, only a single reference level need be used for performing the verification function (e.g., where "0" equals the programmed state, the device only needs to determine whether the cell has reached the "0" state, and can ignore cells targeted to remain in the erased state).

It would be obvious to a circuit designer of ordinary skill to eliminate all but one of the XOR gates (711, 713, 715) in a binary device, since only one bit is being stored in the cell (i.e., "L" = 1). Mehrotra, 342-343; CPX 120; Pathak, Tr. 820-822; CPX 122. In a binary device, it would be obvious to a circuit designer of ordinary skill to change NOR gate 717 to a single inverter, since there would only be a single XOR gate, and therefore only a single input. Mehrotra, Tr. 342-345; CPX 120; Pathak, Tr. 820-822; CPX 122.

Furthermore, in implementing Figure 16 of the `338 patent in a binary device, the possible combinations of read (R) and write (W) are greatly reduced, as compared to a multi-state device, such that it is not necessary to implement the logic inherent in XOR (exclusive OR) gates and NOR gates to verify a cell.[43] Thus, one would expect to make additional simplifications to the circuitry shown in Figure 16 by eliminating entirely the XOR gates and the NOR gate 717. Mehrotra, Tr. 345-351; CPX 120; Pathak, Tr. 819-829; CPX 122; CPX 127; CPX 128. It would be logical to simplify the verification and

[43] There are only four logically possible states: R=0 and W=0; R=0 and W=1; R=1 and W=0; R=1 and W=1. For example, in the first scenario (R=0 and W=0), the data read from the memory is zero (erased) and the data desired to be written into the memory is also zero. Note also that the third scenario (R=1 and W=0) should not be possible because all cells are required to be in an erased state before programming starts. Mehrotra, Tr. 345-346.

inhibit circuitry disclosed in Figure 16 to consist merely of R (where R is the output of the sense amplifier) and the data latch 721, as shown in CPX 127. Mehrotra, Tr. 345-351; CPX 120; Pathak, Tr. 819-829; CPX 122; CPX 127; CPX 128. One familiar with the differences between multi-state cells and binary cells would simplify the verify and inhibit circuitry shown in Figure 16 to the circuitry shown in CPX 127, because such a simplification would reduce the size of the chip, reduce the logic, reduce costs, and give more efficient operation. Pathak, Tr. 829-829.

Based upon the language of claim 27, the specifications of the `338 and `344 patents, as well as extrinsic evidence adduced at the hearing, claim 27 is properly construed to cover a binary device that uses a single sense amplifier to verify whether a cell has reached its programmed state. Furthermore, it would not be logical to construe claim 27 to require the use of a comparator in a binary device. Accordingly, the claim 27 verification means should be interpreted to include the binary simplifications discussed above.

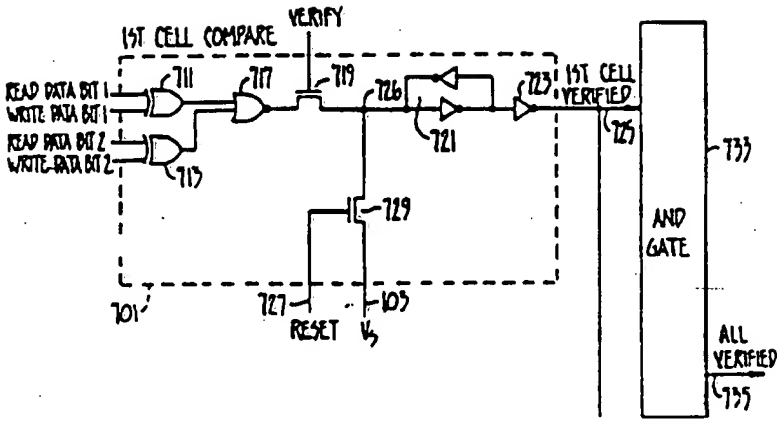
6. The Inhibiting Means

Claim 27 of the `338 patent recites as one of its elements "means for inhibiting further programming of correctly verified cells among the plurality of addressed cells."

Figure 16 of the `338 patent discloses one embodiment of the compare circuit used in the multi-state, preferred embodiment. Figure 16 also discloses circuitry that inhibits further programming of the memory cells. CX 2 at col. 20, line 17-18; Mehrotra, Tr. 340.

The pertinent circuitry is depicted in Figure 16 of the `338 as

follows:[44]



In the circuit shown in Figure 16, a latch 721 performs the function of inhibiting further programming to correctly verified cells. Mehrotra, Tr. 340-342. When a cell is correctly verified, the result is sent to latch 721, which is then set to the verified state. Mehrotra, Tr. 340; CX 2 at col. 20, lines 28-32. The specification mentions that at the end of a programming pulse all the latches are reset to the unverified state. Node 726 can only be reset by transistor 729 and not by node 717 after node 726 goes high. Mehrotra, Tr. 3. Once latch 721 is set in the verified state, the cell is inhibited from further programming during any subsequent programming pulses which may be applied.[45] Mehrotra, Tr. 340.

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[44] The illustration, supra, like the illustration contained in Respondents' Reply brief, depicts the circuitry of one compare module contained in the preferred embodiment (compare module 701). Figure 16 and the text of the specification provide for "N compare modules such as 701, 703, one for each of the N cells in the chunk." CX 2 at col. 20, lines 18-20, Fig. 16.

[45] The '338 patent specification teaches that "[p]rogramming and verification are repeated until all the cells are correctly verified in FIG. 15(7)." CX 2 at col. 20, lines 14-16. Thus, each cell must be read to

(continued...)

Thus, latch 721 in Figure 16 is a "one-way latch." Latches are often referred to as "one-way" or "two way." One-way latches and two-way latches are often drawn in the same manner. Mehrotra, Tr. 372, 397. Yet, they function differently. A two-way latch freely switches back and forth between two states when different input values are applied. Thus, if the input to the latch is a 0, then the value saved in the latch becomes a 0. If a subsequent input is a 1, the latch then saves a 1. Allen, Tr. 1077. However, a one-way latch is said to move in only one direction. Thus, for example in Figure 16, when verification occurs and the latch is set to a 1, the latch does not go back to a zero during the overall cycle of iterations. See Allen Tr. 1078 (for the way a one-way latch works). Thus, a one-way latch like that used in Figure 16 of the `338 patent will not allow the detection of so-called "program disturb conditions" where, due to defects in a part, a cell goes back to an erased state before the entire chunk of data is verified. Nor will a one-way latch allow the detection of conditions in which a part fails and a cell is disturbed from an erase into a programmed state. Harari, Tr. 250-252; Mehrotra Tr. 374-378; CX 2. Furthermore, neither claim 27 of the `338 patent, nor the specification mentions the detection of program disturb conditions.[46]

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[45](...continued)
determine whether the read and write data for that cell match.

[46] Respondents state that Dr. Harari admitted that a device that verifies on an iteration basis would be within the scope of claim 27. See RPRFF 281 citing Harari, Tr. 270. Dr. Harari made the following statement during cross-examination in response to a hypothetical question:

> Q. Well, let me ask you this. If -- if the Samsung device continued to verify, even if it was useless, would you say that it was outside the scope of this claim?
>
> A. No, of course not.

Harari, Tr. 270.

(continued...)

CX 2.

With respect to Figure 16, the specification teaches that the output of the XOR gates passes through NOR gate 717 such that a "1" appears at the output of NOR gate 717 whenever all the bits are verified, otherwise a "0" appears there. When verification occurs (i.e. "[w]hen the control signal VERIFY is true"), "this result is latched to latch 721 such that the same result at the output of NOR gate 717 is also available at the cell compare module's output 725." CX 2 at col. 20, lines 25-32 (emphasis added). The output 725 is fed through an output line to the "program circuit with inhibit 210 of FIG. 5."[47] CX 2 at col. 20, lines 33-36.

The specification in describing the functions of latch 721 states that "[w]hen the control signal VERIFY is true, this result is latched to latch 721." It says nothing about setting latch 721 in case of a subsequent (or previous) control signal VERIFY that is not true. Thus, the specification does not provide that it will return to an unverified state during the program

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[46](...continued)
It is not clear what type of circuitry was assumed by the questioner or what type of circuitry Dr. Harari had in mind when he responded. It is significant that Dr. Harari was asked about a device that somehow continued to "verify, even though it was useless," not about a circuit that continued to apply programming conditions. Claim 27 requires an inhibition against further programming, not further, useless verification. The hypothetical circuit in question did not exclude the fact that it would have an operational program inhibit as required by claim 27.

[47] The program circuit is the circuit that removes voltage from a cell so that further programming (or over-programing) cannot take place. However, as described in the specification, the program circuit depends upon the data latched by latch 721. Although latch 721 is physically contained within the compare module in the preferred embodiment, the results of the comparison of read and write data are latched to latch 721. Latch 721 does not perform that comparison. It plays a role in making sure that correct output is available from the compare module for input to the program circuit.

and verification of a chunk of data.[48] Indeed, since latch 721 is a one-way latch, once the latch is set, the stored data cannot be affected by the output of NOR gate 717. Mehrotra, Tr. 340-341.

The preferred embodiment of the `338 patent is a multi-state device. If latch 721 were not a one-way latch, there would be catastrophic failure of the multi-state device. See McGreivy, Tr. at 1697-1701, 1797-1799; CX 2 at col. 19, lines 4-26. The specification provides that in order to change the setting of latch 721:

> At power-up or at the end of program/verify of a chunk of data, all cell compare module's outputs such as 725, 727 are reset to the "not verified" state of "0". This is achieved by pulling the node 726 to V_{ss} (0 V) by means of the RESET signal in line 727 to a transistor 729.

CX 2, col. 20, lines 46-51.

Thus, the specification teaches that latch 721 must be reset at power up, as well as at the end of each program/verify of a chunk of data. The `338 patent also teaches that before any programming occurs, a read operation must

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[48] Respondents' expert, Dr. Allen, testified at the hearing that latch 721 is a two-way latch. His opinion appears to be based in part on an incorrect reading of the specification text. Referring to column 20, starting at line 28, he testified as follows:

> So we're pointing out that indeed in the language of the specification, the specification calls for on any given iteration within the overall cycle, whatever value is read out on the NOR gate 717 is to be brought over here to the node 725. The only way for that to happen consistently on every iteration as indicated by the language I just read, is for latch 721 to be able to go back and forth. That is to be a two-way latch.

Allen, Tr. 1086 (emphasis added).

However, the specification does not state that whatever value is read out on NOR gate 717 is to be brought over to node 725. As discussed, supra, the specification states in column 20 that the output of NOR gate 717 is available at the cell compare module's output 725 only when the control signal VERIFY is true.

be performed to verify that the read data and the write data match. Thus, if latch 721 were a two-way latch, before the commencement of programming a cell would be read and if found not to be in the correct state, latch 721 would flip back to the not verified state in response to the output of NOR gate 717. A reset operation such as that disclosed in the specification would not be required. Mehrotra, Tr. 399-400. Instead, the specification shows that latch 721 can only be reset by the effect of transistor 729. See Mehrotra, Tr. 342. The specification demonstrates that latch 721, once set to the verified state, remains in the verified state during the entire program/verify of a chunk of data. Then, latch 721 is returned to the "not-verified" state by a reset operation in which node 726 is pulled down, as one would expect in the case of a one-way latch.[49] See Mehrotra, Tr. 400; Allen, Tr. 1079, 1086.

In addition to the disclosure of Figure 16, including latch 721, Figure 5 of the `338 patent contains a block 210 entitled "Program Circuit with Inhibit." This block provides no detail regarding the specific circuitry that actually inhibits further programming. CX 2; Guterman, Tr. 508-510. Figure 17 shows "one embodiment of the program circuit with inhibit 210 of Fig. 5 in more detail." CX 2 at col. lines 52-53. The one embodiment shown in Figure 17 is relevant to the Hot Electron Injection programming method used in the preferred embodiment. The circuitry in Figure 17 is for removing voltage from the drain of a cell to inhibit further programming. CX 2 at col. 20, line 52 through col. 21, line 8; Mehrotra, Tr. 352-353; Guterman, Tr. 511-513. Respondents argue that the means for inhibiting further programming of

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[49] In order to pull down latch 721, one would have to design the circuit shown in Figure 16 to have transistors of the proper size. Allen, Tr. 1079; Mehrotra, Tr. 409. The `338 patent does not indicate the size of the transistors involved in Figure 16. Nonetheless, one of ordinary skill would know how to size the transistors shown in Figure 16 relative to the size of NOR gate 717 so as to achieve a one-way latch. CX 2; Mehrotra Tr. 404-409.

correctly verified cells among the plurality of addressed cells is the program circuit disclosed in Figure 17 of the `338 patent. Respondents' argument with respect to the inhibit means is linked to their argument that HEI programming and a cell that uses such programming must be used in the claimed invention. See Respondents' Post-Hearing Br. at 26-27, RPFF 463-465. This argument has been rejected above in the discussion of the parallel programming means. Furthermore, although the circuitry disclosed in Figure 17 is part of one way of implementing the claimed invention, it depends upon circuity that is actually located with the "compare modules," e.g., latch 721 and compare circuit module output 725.

To one skilled in the art, one way of implementing the inhibit means is to combine certain disclosures in Figures 16 and 5, in particular block 190 of Figure 5, which is entitled "Read/Program Latches and Shift Register." The temporary storage latch disclosed in block 190 of Figure 5 can also serve as the inhibit latch 721 of Figure 16 of the `338 patent. Mehrotra, Tr. 349-351; CPX 120; CX 2, Fig. 16; Pathak, Tr. 835-839; CPX 57C-58C; CPX 124-125. A flash memory designer of ordinary skill would seek to combine the functions of the temporary storage latch and the verify inhibit latch in a single structure in order to save transistors, thereby reducing the surface area of the chip. Pathak, Tr. 839-840.

Consequently, the inhibit means should be interpreted to include a one-way latch 721 or its equivalent.

7. **The Final Means Plus Function Element**

Claim 27 recites as its final element "means for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly."

Complainant argues that this element refers to an iterative process in which the cells are repeatedly verified, utilizing additional programming pulses until all of the addressed cells have been verified. The claimed uniqueness of complainants invention is that the successive programming pulses are applied to only those cells which have not yet been correctly verified (i.e. have not reached their desired state at which point all further programming to already verified cells is permanently inhibited through the remainder of the program cycle).[50]

Respondents argue, however, that Complainant would interpret claim 27 to place an additional "permanently inhibit" limitation on the programming algorithm of the `338 patent. According to Respondents, the `338 device does not permanently inhibit programming of cells that are erroneously verified as correctly programmed. See, e.g., Respondents' Post-Hearing Br. at 14; Respondents' Reply Br. at 12-16.

Figure 16 of the `338 patent discloses structures that correspond to the final means-plus-function element of claim 27 in a multi-state implementation. Those structures include the one-way latch 721, the outputs such as output 725, as well as AND gate 733 whose single output 735 is used to signal the controller in the preferred embodiment that all cells in the chunk of data have been correctly verified. Mehrotra, Tr. 341; CX 2 at col. 20, lines 18-51. Accordingly, the final element of claim 27 should be construed to include these structures or their equivalents.

The parties disagree as to the plain meaning of the patent claim. In particular, there is disagreement as to the effect of the final phrase "until

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[50] OUII agrees with Complainant that "claim 27 is limited to devices which inhibit programming of correctly verified cells for the period of time until all cells are verified correctly." OUII argues that this feature is enabled by latch 721 in Figure 16. OUII Reply Br. at 17 & n.21.

all the plurality of addressed cells are verified correctly." Given the lack of punctuation in the text of the claim and the ordinary meaning of the words contained in that phrase, it appears that the condition specified therein applies to the entirety of the claim language preceding it within the final element, i.e., to both (1) further programming and verifying and (2) inhibiting programming of correctly verified cells. That appears to be the same position taken by Respondents, at least as regards the grammatical function of the final "until ...." phrase contained in the claim element. See Respondents' Post-Hearing Br. at 9-10; Respondents' Post-Hearing Reply Br. at 12.

The Administrative Law Judge reads this final phrase to refer to the fact that the verification and programming process continues until the entire chunk of data is programmed. However, the fact that the final phrase modifies the entire claim element does not require the meaning for the final element proposed by Respondents. Although the final claim element requires further programming until all cells are correctly verified, that does not mean that once a cell is correctly verified that the device must then verify it again and, more significantly, if found no longer to be in the target state that the inhibition against further programming must be removed and the cell must be reprogrammed. Such a limitation is not contained in claim 27, and to construe claim 27 in that manner would ignore the express requirement that programming be inhibited from cells once correctly verified. To construe claim 27 to require that cells which have been correctly verified must be subject to further programming would also be inconsistent with the proper construction of the previous claim element (the inhibiting means), which as discussed above requires a one-way latch like latch 721 in the preferred embodiment or its equivalent.

Furthermore, the description of the means described in the `338 patent specification requires that the programming of each cell be permanently inhibited upon verification.[51] For example, the specification provides in part: "[a]s soon as the programmed state is verified correctly, programming stops." CX 2 at col 18, lines 24-25. The patent provides further that "parallel programming is implemented by a selective programming circuit which disables programming of those cells in the chunk that have already been verified correctly." CX 2 at col. 19, lines 13-16. Finally, the patent also provides that "it is preferable to apply programming voltages in repetitive short pulse with a read operation occurring after each pulse to determine when it has been programmed to the desired threshold voltage level, at which time the programming terminates." CX 2 at col. 9, lines 13-18. Each of the passages clearly indicates that the `338 patent will not apply an additional programming pulse to a cell after it has been verified. See Mehrotra, Tr. 253-254; McGreivy, Tr. 1693-1696.

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[51] Respondents argue that Figure 15 shows that individual cells may be either programmed or inhibited in any individual pulse. See Respondents' Post-Hearing Br. at 4-5; Respondents' Reply Br. at 12; Thomas, Tr. 1510-1511.

Figure 15 is a block diagram that depicts an on-chip program algorithm according to the claimed invention. CX 2 at col 5, lines 42-43, Fig. 5. The algorithm is discussed in the text at col. 19, line 57 through col. 29, line 16. The block at Fig. 15(5) is labeled "Verify Read Data = Program Data For All Addressed Cells." If the answer is "No" the diagram indicates in block 6 that a pulse of program voltage is to be applied only to addressed cells not verified. Respondents interpret this diagram to indicate that each cell must be given an additional programming pulse if upon any verification pulse the cell is found not to be verified correctly. However, Figure 15 cannot be read in isolation. It is given clarity by Figure 16, whose latch 721 operates throughout the programming of a chunk of data to identify a cell as correctly verified once it has reached a programmed state. Thus, a cell once correctly verified will be read as such each time the program algorithm reaches the stage depicted in Fig. 15(5), and in accordance with block (6) such a cell will not receive a further program pulse. Such a cell is permanently inhibited from further programming while the remainder of the chunk of data is programmed.

The distinction between conditional inhibition and termination is an important one. As Dr. McGreivy explained, failure to terminate will, over time, overstress a binary device and make a multi-state device malfunction. McGreivy, Tr. 1697-1708, 1793-1813. This point is addressed in the text of the `338 patent, as follows:

> In the prior art EEprom devices, after each programming step, the state attained in the cell under programming is read and sent back to the controller 140 or the CPU 160 for verification with the desired state. This scheme places a heavy penalty on speed especially in view of the serial link.
>
> In the present invention, the program verification is optimized by programming a chunk (typically several bytes) of cells in parallel followed by verifying in parallel on chip. The parallel programming is implemented by a selective programming circuit which disables programming of those cells in the chunk whose states have already been verified correctly. This feature is essential in a multi-state implementation, because some cells will reach their desired state earlier than others, and will continue pass [sic] [past] the desired state if not stopped. After the whole chunk of cells have been verified correctly, logic on chip communicates this fact to the controller, whereby programming of the next chunk of cells may commence. In this way, in between each programming step data does not need to be shuttled between the EEprom chip and the controller, and program verification speed is greatly enhanced.

CX 2 at col. 19, lines 4-26.

Based upon the plain language of claim 27, the discussion of this issue in the specification, and the disclosure of the one-way latch 721, claim 27 is properly construed to include the limitation of termination or permanent inhibit of programming once a cell has been correctly verified.

IV. VALIDITY

A patent is presumed valid, and the presumption of validity attaches to each claim independently of all other claims. See Jones v. Hardy, 727 F.2d 1524, 1528 (Fed. Cir. 1984); 35 U.S.C. § 282. A party seeking to invalidate a patent must prove facts establishing invalidity by clear and convincing evidence, and the ultimate burden of persuasion never shifts from the patent challenger. Id.; Carella v. Starlight Archery & Pro Line Co., 804 F.2d 135, 138 (Fed. Cir. 1986).

A. The `752 Patent

1. Anticipation

Respondents argue that the U.S. Patent No. 4,931,997 to Mitsuishi et al. anticipates the claimed invention of the `752 patent, thereby making it invalid under 35 U.S.C. § 102(b).[52] Complainant and OUII take the position that the Respondents have not shown by clear and convincing evidence that the `752 patent is invalid.

As discussed below, the Mitsuishi patent does not disclose or teach a "means for selecting a plurality of sectors" because none of its embodiments is capable of selecting a new plurality of sectors for simultaneous erase each time an erase operation is commenced as required by claim 1 of the `752 patent. FF IV 2-18. Nor does the Mitsuishi patent include an "individual register associated with each sector" because it uses a row of the non-volatile memory array, as opposed to a register distinct from the array, to

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[52] 35 U.S.C. § 102(b) provides that one is not entitled to a patent if "the invention was patented ... in this or a foreign country ... more than one year prior to the date of the application for patent in the United States ...."

It has not been disputed that the Mitsuishi patent is prior art against the `752 patent for the purposes of section 102(b).

store permanently the erase status of the memory rows. FF IV 19-32.

With respect to the "means for selecting a plurality of sectors," much of the evidence of record concerns the second embodiment of the Mitsuishi patent. It is the only disclosed embodiment capable of designating more than one row for simultaneous erasure without designating all rows. However, the device disclosed as the second embodiment is a one-time programmable device. FF IV 2-10.

Yet, the text and Figures of the `752 patent corresponding to the means-plus-function element reciting a "means for selecting a plurality of sectors" clearly disclose a device that is capable of selecting a "new" plurality of sectors each time an erase sequence is commenced. CX 1 at col. 5, lines 26-32. The erase algorithm in Figure 4 of the `752 patent clearly demonstrates that each time a new erase operation is commenced in the claimed invention the addresses of all the "new" sectors selected for erase are sequentially loaded into the EEprom system (chip), and the individual register associated with each addressed sector is sequentially "tagged." CX 1, Fig. 4; Mehrotra, Tr. 314. In contrast, the Mitsuishi second embodiment discloses a one-time programmable device that permanently designates rows of memory as non-erasable and stores these permanent designations in the first row of memory in the EEprom array. FF IV 5-13. The second embodiment of Mitsuishi does not disclose any means for altering the identity of any of the erase inhibited rows. FF IV 8-9.

Indeed, the structure (and the corresponding manner of operations) of the second embodiment of the Mitsuishi patent differs substantially from the structures disclosed in the `752 patent which correspond to the "means for selecting" element of claim 1. The preferred embodiment of the `752 patent uses the circuitry shown in Figure 3A of the patent to select the plurality of

sectors selected for erase by sequentially "tagging" the individual registers associated with each selected sector. CX 1 at col. 5, lines 26-32. This selection process occurs each and every erase operation. However, the second embodiment of the Mitsuishi patent shifts the permanently stored information in the first row of the memory array into the column latches to identify the protected rows of memory that will be inhibited from erasure. FF IV VI. No pointing or tagging operation of individual registers takes place.

Samsung argues that the first and second embodiments of the Mitsuishi patent would be merged together by an individual of ordinary skill in the relevant art. Hypothetically such a device would in the very short-run mimic the operation of the device disclosed in claim 1 of the `752 patent. FF IV 14-17. However, the first and second embodiments of the Mitsuishi patent are incompatible and mutually exclusive. FF IV 14-18.

The first embodiment of the Mitsuishi patent discloses a device that erases either a single row or the entire memory chip while preserving the contents of the row in the column latches so that the preserved data can be rewritten into the "protected" row at the end of the erase operation. FF IV 2. In contrast, the second embodiment of the Mitsuishi patent discloses a device that inhibits the erasure of the permanently designated rows of memory, while bulk erasing all non-inhibited rows. FF IV 5. In the second embodiment, the identity of the protected rows are permanently stored in the first row of the memory array. FF IV 6-11. There is no disclosure in the Mitsuishi patent that would permit a user to rewrite the data in row 11 to alter the identity of the erase inhibited rows. FF IV 9. Moreover, there is no suggestion in the Mitsuishi patent to an individual of ordinary skill that

these two embodiments could be combined. FF IV 14-17.[53] Indeed, the third embodiment of the Mitsuishi patent, which discusses both the first and second embodiments, clearly indicates the opposite. FF IV 16.

Samsung's contention that the Mitsuishi Patent anticipates the "means for selecting a plurality of sectors" in claim 1 of the `752 patent is based on its erroneous conclusion that the "normal" operation of the second embodiment of the Mitsuishi patent permits the contents of row one to be reprogrammed.[54] However, there is no disclosure in the Mitsuishi patent to indicate that the second embodiment can select a new plurality of rows for

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[53] Each row of nonvolatile memory has a limited operating life. If a row from the non-volatile memory array of a EEprom chip were used to store the erase status of each row in the array, as all of the embodiments of the Mitsuishi patent teach, the resulting device, if reconfigurable for each erase operation, would have a very limited useful life and would be unusable as the EEprom system claimed in claim 1 of the `752 patent because row 11 would have to be erased and rewritten each time a new row is selected for erase. An individual of ordinary skill would not design a `752 patent mass storage device that uses a row from the nonvolatile memory array to store the erase status of each row in the array. It would be illogical and would not be done. It would be an inefficient and wasteful use of silicon. FF IV 17-22.

Additionally, the stated objectives of the `752 patent include "provid[ing] a Flash EEprom memory system with enhanced performance and which remains reliable after enduring a large number of write/erase cycles" and "minimiz[ing] stress to the Flash EEprom device." CX 1 at col. 1, lines 34-44, 51-53. In a mass storage context, the hybrid device proposed by Samsung would have the exact opposite effect. FF IV 19-20. The Mitsuishi architecture greatly increases the stress on an EEprom device because the data in row 11, which stores the erase status of each row in the array, must be erased and rewritten each and every time any row in the array is to be selected for erase. FF IV 20. This constant erasing and rewriting of row 11 would quickly over-stress the proposed Mitsuishi hybrid and guarantee a very short operating life for the device. FF IV 19-20. Furthermore, the circuitry necessary to implement the hybrid device into a modern EEprom array would discourage any attempt to build a `752 patent-like device because the amount of circuitry necessary would consume an excessive amount of the silicon area. FF IV 22. Such circuitry would in any event be limited to square array architectures which are impractical in large arrays of the sort disclosed in the `752 patent. FF IV 23.

[54] Row one is the portion of the memory array that stores the addresses of rows inhibited from erasure. FF IV 6.

protection from erase by rewriting the contents of row one. FF IV 5-18. As disclosed in the Mitsuishi Patent, all erase operations for the second embodiment are performed under bulk erase (or AS=1) conditions.[55] Under these conditions, the data in row one of the Mitsuishi memory array is fixed, and the device cannot select any new combination of rows for protection from erase. FF IV 6-18, 29.[56]

The Mitsuishi Patent specifications simply do not support Samsung's contention that the normal operation of the second embodiment permits a user to send an external command to the device to shift the erase mode from bulk erase (AS=1) to single row erase (AS=0) so that any row of the memory array (including row one) can be erased and rewritten. FF IV 7, 11, 29. On the contrary, the Mitsuishi Patent indicates that the two erase modes (bulk and single row) cannot exist in the same device.[57] FF IV 14-17.

With respect to "individual register" required by claim 1 of the `752 patent, the Mitsuishi patent lacks this element because the "individual register" claim of claim 1 of the `752 patent must be a resettable circuit comprised of one or more latches that is separate from the memory array. FF IV 19-26.

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[55] AS is the internal signal of the Mitsuishi Patent that indicates whether or not a global erase operation will be performed on the EEprom chip. When AS=1, all non-inhibited rows of the memory array are simultaneously erased. FF IV 5.

[56] In fact, even Samsung concedes that the second embodiment does not anticipate claim 1 when the device operates under the condition where internal signal AS is set to "1" (indicating that the device bulk erases the entire chip minus the protected row). FF IV 5. However, AS=1 is the sole operating condition for the second embodiment of the Mitsuishi Patent.

[57] The second embodiment does not permit the data in the first row of the EEprom array to be altered because the exclusive function of the second embodiment is to prevent the illicit or unlawful modification of data within the protected rows of the Mitsuishi Patent EEprom device. FF IV 14-17.

The ability to set and reset (i.e., tag and untag) individual registers is an essential feature of claim 1 because the invention mandates that the claimed EEprom system possess the capability of selecting new combinations of sectors each time an erase operation is commenced. CX 1 at col. 5, lines 26-32. During an erase operation, the function of the individual register is to indicate whether or not its associated sector has been selected for erase. CX 1 at col. 17, lines 1-3. If a sector has been selected or "tagged" for erase, the individual register is set "high." CX 1 at col. 5, lines 26-32. If the sector has not been selected for erasure, the individual register is "low" to indicate the "untagged" status of its associated sector. Id. Thus, for any given erase operation, the individual register must be capable of indicating either erase status ("selected" or "unselected") for its associated sector. Id.; CX 1 at col. 17, lines 1-3.

In contrast, the latches in the second embodiment of the Mitsuishi patent, which Samsung asserts are equivalent to the claimed individual registers, permanently designate the rows of memory that are inhibited from erasure. FF IV 5-13. Each of these latches operate like one-time programmable circuits because in operation they permanently indicate one and only one erase status ("always erase" or "never erase") for their associated rows of memory. Id. It has not been shown that for the purposes of an erase operation these latches are resettable and thus capable of holding a different value ("0" or "1") each time the device commences a new erase operation. See FF IV 19-26.

Furthermore, in the Mitsuishi patent the "individual registers" do not consist of "one or more latches," but necessarily include row 11 of the memory array. Id. Since the column latches in Mitsuishi are not dedicated or "individual" (in the sense of the `752 patent) to each row, they necessarily

require the data stored in row 11 of the memory array to identify the rows of memory to be protected from erasure. FF IV 6. This is a completely different structure which behaves in a completely different way from the individual registers of the `752 patent. As explained above, no "pointing" to individual sectors takes place, and the Mitsuishi structure would quickly run out of endurance if forced into a true multisector erase device as disclosed in the `752 patent. FF IV 6, 13; but see CX 1 at col. 5, lines 26-32.

Accordingly, for the above reasons, it has not been shown by clear and convincing evidence that the Mitsuishi patent anticipates claim 1 of the `752 patent.

For the reasons stated above, the Mitsuishi patent cannot anticipate dependent claims 2 or 4 of the `752 patent because it does not possess the element of independent claim 1 reciting a "means for selecting a plurality of sectors," nor does the Mitsuishi patent include the elements of claims 1, 2 and 4 reciting an "individual register associated with each sector."

2. Obviousness

Respondents argue that the Mitsuishi patent combined with other references make the claimed invention of the `752 patent obvious,[58] and therefore invalid under 35 U.S.C. § 103.[59] Complainant and OUII take the

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[58] Based on Respondents' Post-Hearing Brief and Proposed Conclusions of Law, it appears that Respondents take the position that the entire `752 patent is invalid for obviousness.

[59] Section 103 of the Patent Act provides in pertinent part as follows:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

(continued...)

position that Respondents have not shown by clear and convincing evidence that the `752 patent is invalid.

In order to prove invalidity under section 103 of the Patent Act, it must be demonstrated by clear and convincing evidence that the claimed invention would have been obvious in light of the combined teachings of items of prior art relied by Respondents. See Graham v. John Deere Co., 383 U.S. 1, 37 (1966); Jones v. Hardy, 727 F.2d 1524, 1530-32 (Fed. Cir. 1984); Litton Sys., Inc. v. Honeywell, 97 F.3d 1559, 1566 (Fed. Cir. 1996) (section 103 obviousness analysis requires a determination of the scope and content of the prior art, the differences between the prior art references and the claimed invention and the secondary indicia of nonobviousness). In addition, it must be shown that one of ordinary skill would have known to combine these items. See Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1050-1051 (Fed. Cir. 1988).[60] As discussed below, the required showing has not been made to find

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[59](...continued)
35 U.S.C. § 103(a).

[60] An individual of ordinary skill in the art of flash memory has at least a bachelor's degree in a field such as electrical or computer engineering (or experience equivalent thereto) and at least a few years of work experience with EEproms. FF IV 167-172. The level of ordinary skill in the art is the same for the `752 and `338 patents. FF IV 173.

Respondents' expert conceded that the level of ordinary skill for the Mitsuishi patent and the `752 patent is the same. FF IV 93. However, Respondents argue that the level of ordinary skill in the art for the `338 and `752 patents is not the same. They argue that an individual of ordinary skill in the art of the `338 patent would need to possess an understanding at an operational level of how the memory cells would be used as circuit elements in the overall memory design, which would not be required for an individual of ordinary skill in the art of the `752 patent. RPRF 431; Allen, Tr. 1119. Yet, Complainant's expert, who has had extensive experience with the commercial design and manufacture of EEprom devices and with individuals typically involved in such work explained that one of ordinary skill, as it pertains to the `752 patent, would have to have an understanding of digital logic, some degree of knowledge about testing, an understanding of specifications and an understanding of the characteristics of mass storage
(continued...)

any claim at issue of the `752 patent obvious in view of the prior art.

Samsung argues that the `752 patent was rendered obvious by a combination of the Mitsuishi patent, U.S. Patent No. 4,752,871 (the "Sparks Patent"), U.S. Patent No. 4,099,069 (the "Cricchi Patent"), and an article by Colin S. Bill entitled "A Temperature and Process-Tolerant 64K EEPROM" (the "Bill Article").[61]

None of the prior art cited by Samsung suggest the elements of the `752 patent claiming a "means for selecting a plurality of sectors" or an "individual register associated with each sector." See FF IV 11-24, FF IV 35-54.

The Mitsuishi patent was discussed in detail above. It does not disclose crucial features of the claimed invention. For example, with respect to independent claim 1 of the `752 patent, the Mitsuishi patent does not teach or disclose in any way a "means for selecting a plurality of sectors" or "individual register associated with each sector."

The Sparks patent was considered by the Patent Examiner during the prosecution of the `752 patent. CX 1, "References Cited." In the `752 patent, all the sectors within an array are linked together. It is impossible to read one sector while erasing another. Because each array in the Sparks patent operates like a separate chip, the Sparks patent does not suggest the concept of dividing a single array into a plurality of individually addressable sectors. Thus, the Sparks patent does not disclose a means for selecting a plurality of sectors. FF IV 52-54.

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[60](...continued)
systems. McGreivy, Tr. 1643-1653.

[61] It has not been disputed that these references constitute prior art to the `752 patent for the purposes of a validity analysis under section 103.

In the Sparks patent, each EEprom subarray has its own data bus and operates like a separate EEprom chip. Yet, in the `752 patent, all the sectors within an EEprom array share the same interface/data bus. FF IV 47. In the Sparks patent, each EEprom array is completely independent of each other. The Sparks patent permits the device to read the data from one array while simultaneously bulk erasing the data located on a separate array. FF IV 47. There is no disclosure in the Sparks Patent suggesting that each EEprom array should be subdivided into a plurality of sectors with each sector having an individual register for holding its erase status. FF IV 50. Thus, the Sparks patent does not disclose an individual register associated with each sector.

The Cricchi Patent does not provide any disclosure that the described EEprom device must be capable of storing more than one address at a time for erase operation. Thus, the Cricchi Patent does not disclose a means for selecting a plurality of sectors. FF IV 42.

The Cricchi Patent does not provide any disclosure regarding the addressing logic used to select a block of memory for erase. FF IV 39. The Cricchi Patent does not provide any structure or manner for storing the addresses of selected blocks prior to commencing the erase operation. The Cricchi Patent does not disclose the use of an individual register associated with each block. FF IV 41.

In the Bill Article, the disclosed device is incapable of simultaneously writing (or erasing) bytes in two different pages within the array. FF IV 37. The Bill Article does not disclose the function of (or corresponding structure for) selecting a plurality of sectors. RX 67.

In addition to the fact that none of the prior art cited against the `752 patent discloses or suggests substantial portions of the claimed

invention, there is no evidence that a person of ordinary skill would have known to combine these references. Nor is there evidence to support a finding that there was something in the cited art that would suggest to an individual of ordinary skill that the above pieces of art should be combined to build a device that practices the claims of the `752 patent. See Id. IV 34.

Furthermore, there are secondary indicia of the validity of the `752 patent. The `752 patent has played a crucial role in SanDisk's success because it gives SanDisk products superior performance and endurance. FF IV 55. Prior to the `752 patent there was a need for a mass storage system to emulate a disk drive that would be fast and have a long product life. Erase stress is reduced by having the capability of individually selecting which sectors will be erased. Multisector erase also increases the erasing speed of the EEprom device. FF III 107, IV 65.

Intel Corporation ("Intel"), the world's largest commodity flash memory producer, entered into a licensing agreement for all of SanDisk's patents, including the `752 and `338 patents. FF IV 200.

Accordingly, it has not been shown by clear and convincing evidence that the prior art cited against the `752 patent makes the claimed invention obvious under section 103.

3. Best Mode

Respondents argue that the `752 patent specification fails to disclose the best mode contemplated by the inventors of carrying out the claimed invention as required by 35 U.S.C. § 112, ¶ 1, and therefore the `752 patent is invalid. Complainant and OUII take the position that Respondents have not shown by clear and convincing evidence that the `752 patent is invalid.

The patent laws require the specification to "set forth the best mode contemplated by the inventor of carrying out his invention."[62] 35 U.S.C. 112.

The Court of Appeals for the Federal Circuit set forth the best mode requirement, as follows:

> In short, a proper best mode analysis has two components. The first is whether, at the time the inventor filed his patent application, he knew of a mode of practicing his claimed invention that he considered to be better than any other. This part of the inquiry is wholly subjective, and resolves whether the inventor must disclose any facts in addition to those sufficient for enablement. If the inventor in fact contemplated such a preferred mode, the second part of the analysis compares what he knew with what he disclosed -- is the disclosure adequate to enable one skilled in the art to practice the best mode or, in other words, has the inventor "concealed" his preferred mode from the "public"? Assessing the adequacy of the disclosure, as opposed to its necessity, is largely an objective inquiry that depends upon the scope of the claimed invention and the level of skill in the art.

Chemcast Corp. v. Arco Indus. Corp., 913 F.2d 923, 927-28 (Fed. Cir. 1990)(emphasis in original).

Thus, the best mode inquiry has subjective and objective components. The best mode inquiry presents a "subjective, factual question" as to "the inventor's state of mind as of the time he filed his application" with respect to the best mode contemplated by him for carrying out his invention. Id. at 926. "[T]he level of skill in the art and the scope of the claimed invention

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[62] The first paragraph of section 112 of the Patent Act provides as follows:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

35 U.S.C. § 112, ¶ 1.

[are] additional, objective metes and bounds of [the] best mode disclosure."[63] Id.

Although the inventor's state of mind as to the contemplated best mode must be determined, state of mind is not the focus of the inquiry as to whether or not the best mode was concealed in the patent application. A "concealment" of the best mode may occur accidentally or intentionally. Spectra-Physics, Inc. v. Coherent, Inc., 827 F.2d 1524, 1535 (Fed. Cir.), cert. denied, 484 U.S. 954 (1987).

A patent disclosure is not a "product specification," and thus technical details apparent to a person of ordinary skill need not be included in the patent specification. The best mode inquiry is directed to what the applicant regards as the invention, which in turn is measured by the claims. Unclaimed subject matter is not subject to the disclosure requirements of § 112. Engel Indus. Inc. v. Lockformer Co., 946 F.2d 1528, 1531 (Fed. Cir. 1991).

A failure to comply with the best mode requirement must be shown by clear and convincing evidence. Id.

Respondents argue that Mr. Mehrotra, one of the named inventors, considered a charge pump to be the "best mode" for practicing the `752 patent. It is argued that `752 patent fails the best mode requirement because SanDisk did not disclose the use of a charge pump to connect the erase voltage and the outputs of the selected registers to pass on the high voltage to the erase gates of the selected sectors. In particular, Respondents rely on the fact that named inventor "Mehrotra testified that as of the filing date of the `752 patent, SanDisk had designed a 288K test chip and a 4K device that

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[63] The Federal Circuit has held that "[n]otwithstanding the mixed nature of the best mode inquiry, and perhaps because of our routine focus on its subjective portion, we have consistently treated the question as a whole as factual." Chemcast Corp., 913 F.2d at 928.

incorporated the subject matter of claims 1, 2 and 4 of the patent. RFF 659." Respondents' Post-Hearing Br. at 32. Indeed, Mr. Mehrotra testified that at the time the `752 patent application was filed SanDisk was developing test products which incorporated multi-sector erase, and that SanDisk considered the use of a charge pump for these devices. FF IV 76, 79.

Yet, the techniques and circuitry used to generate and apply the erase voltage to the selected sectors are not part of the claimed invention of the `752 patent. See FF IV 66-74. The `752 patent is a logic level patent which was not meant to be limited to any particular type of flash memory cell or technology. FF IV 95. The `752 patent is applicable to various technologies and cells.

Inventors Harari and Mehrotra both testified that they did not consider the actual structure used to generate and apply the erase voltage to the selected sectors to be part of the inventive feature of the `752 patent, nor did they consider it to be part of the means for simultaneously performing the erase operation. FF IV 74, 75. The inventors did not in fact contemplate a best mode for connecting the erase voltage and the outputs of the selected registers.

Respondents assert that the charge pump "falls within the scope of the Harari `752 patent because it is necessary to achieve the functionality recited in claims 1, 2 or 4." Respondents' Post-Hearing Br. at 33.[64] However, the function claimed in the element which requires a "means for simultaneously performing the erase operation on only the plurality of selected sectors," is the ability simultaneously to erase selected sectors,

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[64] The power supply, system software and microprocessor are necessary to "achieve the functionality" of the claims, and yet it is not argued that they are part of the claimed invention.

not the generation of the erase voltage. See discussion above on claim construction; FF IV 81; see also SPFF 392.

Nevertheless, even assuming the physical scheme for applying the erase voltage to the selected sectors were within the scope of the `752 patent, there is no clear and convincing evidence that the `752 inventors concealed a best mode. The `752 patent is broad enough to cover numerous flash memory technologies. See FF IV 66, 73. The specific physical scheme used to erase a sector of flash memory is determined by the flash memory technology chosen. FF IV 67; see SPFF 377. For example, some flash memory devices erase a cell by applying high voltage to the erase gate of the cell to pull electrons off the floating gate. FF IV 68, 69. In contrast, other flash memory devices use a low or negative voltage in their erase operations. For such devices, CMOS logic circuits, resistor networks, depletion load transistors or even charge pumps can be used to accomplish the erase. FF IV 70. One of ordinary skill in the art of the `752 patent would know, depending on the type of cell technology being used, what type of circuit or structure to use in order to generate and apply the erase voltage to the sector for erasure of the cells. FF IV 71, 72. The techniques and circuitry for generating and applying erase voltage either to a single block or to the entire chip were well known in the art.[65] FF IV 71, 81, 82.

A patent need not teach, and preferably omits, that which is well known in the art. Hybritech, Inc. v. Monoclonal Antibodies, Inc., 802 F.2d 1367,

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[65] Respondents argue that "SanDisk presented no evidence that the use of the charge pump was a product specification, a routine manufacturing choice, or was based simply on commercial efficiency." Respondents' Post-Hearing Br. at 33. However, SanDisk has presented such evidence. As stated, supra, the specific circuitry used to generate and apply the erase voltage to the selected sectors depends entirely on factors outside the scope of the `752 patent. FF IV 67; see SPFF 377, 382.

1384 (Fed. Cir. 1986), cert. denied, 480 U.S. 947 (1987). Here, the evidence establishes that the techniques and circuitry used to generate and apply the erase voltage to the selected sectors were well known in the art at the time the application for the `752 patent was filed. FF IV 66-72; see SPFF 375, 377, 381-83, 397, 400, 401. Furthermore, the evidence establishes that one of ordinary skill in the art would know how to employ the various structures. Id.

Therefore, there is not clear and convincing evidence that the `752 patent (particularly the claims at issue) is invalid for failure to disclose the best mode as required by 35 U.S.C. 112, ¶ 1.

4. Enablement

Respondents argue that the disclosures of the `752 patent do not enable one of ordinary skill to implement the claimed invention, as required by 35 U.S.C. 112, and that therefore the `752 patent is invalid. Complainant and OUII take the position that Respondents have not shown by clear and convincing evidence that the `752 patent is invalid.

The first paragraph of 35 U.S.C. § 112 requires the specification of a patent to "contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same." Whether a patent is enabling is a question of law. Raytheon Co. v. Roper Corp., 724 F.2d 951, 951-60 (Fed. Cir. 1983), cert. denied, 469 U.S. 835 (1984). Invalidity on grounds of non-enablement must be proven by facts supported by clear and convincing evidence. U.S. v. Telectronics, Inc., 857 F.2d 778, 785 (Fed. Cir. 1988), cert. denied, 409 U.S. 1046 (1989).

The test of enablement is whether one reasonably skilled in the art

could make or use the invention from the disclosures in the patent, coupled with information known in the art, without undue experimentation. Telectronics, 857 F.2d 778, 785. A patent need not teach, and preferably omits, that which is well known in the art. Hybritech, 802 F.2d at 1384. Indeed, an inventor is not required to describe every detail of his invention in the specification. In re Hayes Microcomputer Products, Inc., 982 F.2d 1527, 1534 (Fed. Cir. 1992) (emphasis added). For example, the description of an apparatus with block diagram describing the function, but not the structure, of the apparatus may be enabling as long as the structure is conventional and can be determined without an undue amount of experimentation. In re Ghiron, 442 F.2d 985, 991 (C.C.P.A. 1971).

Respondents argue that "the `752 patent nowhere depicts or describes how the outputs of the erase enable registers and the AND gate connect to the memory cells of the array." Respondents' Post-Hearing Br. at 35.

Respondents' argument is directed toward the physical scheme for actual erase of the memory cells within a selected sector, which is not part of the claims of the `752 patent. The `752 patent teaches an on-chip circuit structure that is capable of selecting multiple sectors for erase prior to simultaneously erasing the selected sectors. See Guterman, Tr. 434. As explained above, the process and circuitry actually used to erase a sector of flash memory were well known in the art at the time the `752 patent application was filed. Moreover, the particular structure used for supplying the erase voltage and the type of device used to apply the erase voltage selectively to the sectors depend on the type of cell technology used and do not fall within the claims of the `752 patent. See FF IV 67-72, 83. Consequently, such structures need not be disclosed in order for the patent to be enabling.

In addition, Respondents' argument concerning the alleged lack of enablement by the `752 patent is inconsistent with the testimony of their expert concerning the Mitsuishi patent. During the hearing, Respondents' expert, Dr. Allen, testified that a person of ordinary skill in the art that pertains to the Mitsuishi patent has the same level of skill as that which pertains to the `752 patent. FF IV 92. He further testified that the Mitsuishi patent disclosure provides enough information to enable one of ordinary skill in the art to construct a EEprom system as disclosed in the `752 patent. FF IV 93. He also admitted that the Mitsuishi patent discloses no circuit mechanism for generating an erase voltage. Id. Indeed, he admitted that one of ordinary skill in the art of the `752 patent would know to use AND circuitry to combine the two signals to erase the sectors.[66] FF IV 95. Neither the Mitsuishi patent nor the `752 patent discloses a mechanism for generating or applying the erasing voltage to the selected sectors because such techniques were well known in the flash memory art at the time the `752 patent was filed. See FF IV 85-91.

In view of the evidence relevant to this issue, it is clear that there is not clear and convincing evidence that the `752 patent is invalid for lack of an enabling disclosure.[67]

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[66] At one point in his testimony, Respondents' expert stated that one of ordinary skill given the `752 patent would not know enough to build the device described therein because it uses "non-standard voltages" to perform the erase operation. Allen, Tr. 1128-1129. Such concerns over "non-standard voltages" did not, however, prevent him from further testifying that the `752 patent was fully anticipated by the Mitsuishi patent (which does not disclose any structure for generating erase voltage), and that the Mitsuishi patent contains sufficient information to enable one to build the device described in the `752 patent. FF IV 92-93; see SPFF 343.

[67] In connection with the `752 patent, Complainant and OUII expected Respondents to raise an issue of alleged indefiniteness, under 35 U.S.C. § 112. Complainant and OUII persuasively briefed the issue, arguing that the (continued...)

B. The `338 Patent

Samsung's on-sale bar, anticipation and obviousness affirmative defenses against claim 27 of the `338 patent depend on its argument that the claim covers EEprom devices that inhibit the programing of correctly verified cells for only one iteration. As discussed in detail above, Samsung's proposed construction of claim 27 has not been adopted. It has been found as a matter of law that claim 27 requires permanent inhibition of further programming pulses to a cell that has been verified during the programming of a chunk of data. Consequently, Samsung has not in connection with its affirmative defenses established by clear and convincing evidence that claim 27 of the `338 patent is invalid.

1. On-Sale Bar

Respondents argue that a television tuner manufactured by SGS Thomson, and identified as the M293 device, anticipates claim 27 of the `338 patent, and acts as an on-sale bar under 35 U.S.C. § 102(b), thereby making claim 27 invalid.[68] Complainant and OUII take the position that Respondents have not shown by clear and convincing evidence that the claim is invalid.

In order to establish an on-sale bar, the Samsung Respondents have the burden of demonstrating by clear and convincing evidence that each element of claim 27 is embodied in the M293 device. See Ferag AG v. Quipp, Inc., 45 F.3d

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[67](...continued)
`752 is not deficient in that regard. However, Respondents did not raise this issue in their briefs, and the issue is therefore abandoned. See OUII's Reply Br. at 14 n.18.

[68] Under 35 U.S.C. § 102(b), "[a] person shall be entitled to a patent unless the invention was . . . in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States."

1562, 1566 (Fed. Cir.), cert. denied, 116 S.Ct. 71 (1995).[69] However, the evidence of record shows that the M293 device does not perform the claimed function of permanently inhibiting the programming of correctly verified cells "until all the plurality of addressed cells are verified correctly" and therefore cannot act as an "on-sale bar" under 35 U.S.C. § 102(b).

Exemplars of the M293 device were the subject of testing performed during the course of this investigation in order to determine whether the device embodies each of the elements of claim 27 of the `338 patent. Particular emphasis was placed on the device's ability to inhibit programming pulses to correctly verified cells. The testing performed on behalf of Respondents is reflected in the TAEUS Report (RX 180C). SanDisk performed its in-house tests and submitted a Report (CX 199). Testing that was agreed to by both SanDisk and Samsung is reflected in the Chipworks Report (CX 204). Although TAEUS, SanDisk and Chipworks used different testing protocols and conditions, each demonstrated that the M293 device is not capable of permanently inhibiting programming of correctly verified cells as required by claim 27 of the `338 patent.

The TAEUS Report submitted by Samsung shows that the circuitry of the M293 device lacks any structure capable of permanently inhibiting the correctly verified cells from further programming. FF IV 101-102. The M293 test Report submitted by SanDisk, as testified to by Mr. Mehrotra of SanDisk, establishes that the M293 device does not perform the function of permanently inhibiting the programming of verified cells until all the plurality of addressed cells are verified correctly, and does not have the structure to do so. FF IV 98-102. Furthermore, the Chipworks Report also shows that the M293

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[69] SanDisk does not dispute that the SGS device was on sale in the United States more than one year before the `338 patent application was filed.

device does not permanently inhibit the correctly verified cells from further programming, or contain circuitry necessary to meet that claim limitation. FF IV 123, 133, 140.

The most significant differences between the M293 device and the structure and the function required by claim 27 are due to the fact that the verification and inhibiting circuitry of the M293 does not include a "one-way" latch that terminates the programming of a cell upon verification. See FF IV 102. Consequently, unlike the invention claimed in the `338 patent, the M293 device only inhibits verified cells on a temporary or conditional basis. FF IV 101.

For example, if a particular bit verifies as programmed after the third programming pulse in the M293 device, it will be inhibited from programming on the fourth pulse. However, since each cell is reverified after each subsequent programming pulse, if the cell should then fail the verification step following the seventh programming operation (e.g., because it was a borderline pass or because an error occurred in the read/verify step), the cell will then receive an additional programming charge during the eighth programming pulse. Gross, Tr. 1453-1454. Thus, the M293 device does not inhibit "programming of correctly verified cells until all the plurality of addressed cells are verified correctly." See FF IV 99.

In addition to proposing a different interpretation for claim 27, Samsung argues that the M293 performs the claimed function of terminating the programming of verified cells because in "normal operation" the device will not apply an additional programming pulse to a cell that has been already verified.

Samsung contends that the additional programming pulses issued to already verified cells during Chipworks testing of the M293 device is

attributable solely to variations in the input voltage and the capacitive loading of the equipment. However, Chipworks concluded that this could not be the case for at least certain of the wave forms generated during testing. See FF IV 145-152.

Furthermore, the purpose of the permanent inhibit function of the `338 patent is to prevent the application of a programming pulse to a cell in those situations where the device experiences a misread or false verify.[70] See McGreivy, Tr. 1697-1708; section on claim construction. Thus, Samsung's argument concerning supposedly normal operations of the M293 does not show that the device contains all the elements of claim 27 of the `338 patent.

Therefore, for the reasons stated above, sales of the SGS M293 device did not act as an on-sale bar to the patentability of claim 27 of the `338 patent.

2. Anticipation (the Torelli Article)

Respondents argue that an article by Guido Torelli, et al., entitled "An Improved Method for Programming a Word-Erasable EEPROM" (the "Torelli Article")((RX 71) anticipates claim 27 of the `338 patent, thereby making the claim invalid.[71] See FF IV 153. The Torelli Article describes the operation and characteristics of the M293 device. FF IV 154. Complainant and OUII take

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[70] Such occurrences take place under normal conditions without the presence of any testing equipment. See Allen, Tr. 1177.

[71] Respondents' arguments concerning alleged anticipation by the Torelli Article are based on Section 102(b) of the Patent Act, which provides that a person is not entitled to a patent if:

> the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States ....

35 U.S.C. § 102(b).

the position that Respondents have not shown by clear and convincing evidence that the claim is invalid.[72]

In order for the Torelli Article to anticipate claim 27 of the `338 patent, it must be proven by clear and convincing evidence that "all of the elements and limitations of the claim are found within [this] single prior art reference." Scripps Clinic & Research Found. v. Genentech, Inc., 927 F.2d 1565, 1577 (Fed. Cir. 1991).[73]

As in the case of the M293 device, the Torelli Article does not disclose the function of permanently inhibiting the programming of verified cells. FF IV 154-160. Figure 4 of the Torelli Article and its associated text show that all the cells being programmed are "read/verified" between each and every programming pulse. FF IV 157-158.[74] At trial, all the witnesses uniformly agreed that the M293 device discussed in the Torelli Article does not perform the claimed function of permanently inhibiting the programming of correctly verified cells. FF IV 154-155, 99-102, 151-160. Indeed, there is no structure disclosed or suggested in the Torelli Article, such as a one-way

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[72] Prior to the hearing, the Administrative Law Judge was informed that Complainant and Respondents sought reexamination of the `338 patent in light of the Torelli Article, and SGS brochures and technical notes. The Administrative Law Judge did not believe it suitable to suspend this investigation based on the particular circumstances existing in this case, including: the fact that the hearing was imminent and the parties had virtually completed preparations for the hearing; the lack of detailed statements from the PTO concerning the effect of the Torelli Article or other references on the `338 patent; and the likelihood of a substantial period of time before a definitive decision would be made by the PTO.

[73] It was not disputed that the Torelli Article was published early enough so that it could be cited against the `338 patent under section 102(b).

[74] In fact, the related M293 device will apply a programming pulse to a cell whenever that cell is read by the device to be in the unprogrammed state regardless of whether it was verified and inhibited during the application of a previous programming pulse. FF IV 154-155, 159-160, 165.

latch, to track whether a cell was verified/inhibited during the application of a previous pulse so as to disable any further programming of that cell. FF IV 159-160.

In addition to the dispositive absence of the termination function, it has not been established that the Torelli Article contains sufficient disclosures of structures required to perform other functions required by claim 27.

The Torelli Article does not disclose any structure for temporarily storing a chunk of data for programming a plurality of addressed cells. FF IV 161. Although one may infer that there is a location for temporarily storing data, it is not clear from the article whether temporarily stored data is to be stored on or off chip. FF IV 162; McGreivy, Tr. 1759-1763.

The Torelli Article does not disclose any structure for verifying the programmed data in each of the plurality of addressed cells with a chunk of stored data. Without further disclosure in the article, one of ordinary skill in the art would not know the type of structure to use for the verification function. FF IV 166.

Finally, the Torelli Article does not disclose any structure for further programming and verifying in parallel the plurality of addressed cells and inhibiting the programming of verified cells until all the plurality of addressed cells are verified. The article does not disclose the type of verification and program inhibit functions required by claim 27 of the `338 patent, let alone a means for continuing such functions until all the plurality of addressed cells are verified. See FF IV 165, 166.

Aside from the failure by the Torelli Article to disclose these elements required by claim 27 of the `338 patent, the insufficiency of disclosure would also deny an individual of ordinary skill the ability to build the device

disclosed in claim 27 of the `338 patent. FF IV 159-166. Consequently, the lack of enablement by the Torelli Article prevents it from anticipating claim 27 of the `338 patent, independently of its failure to disclose the program inhibit element. See Akzo N.V. v. United States Int'l Trade Comm'n, 808 F.2d 1471, 1479 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987) (in order to anticipate a claimed invention, a prior art reference must be enabling, thus placing the allegedly disclosed matter in the possession of the public).

Given the total absence in the Torelli Article of key structures and limitations required by the patent claim, it has not been shown by clear and convincing evidence that the Torelli Article anticipates claim 27 of the `338 patent.

3. Obviousness

Respondents argue that the Torelli article and the devices and product literature (SGS data books and technical notes) based on it render the claimed invention of the `338 patent obvious under 35 U.S.C. § 103, and therefore invalid.[75] Complainant and OUII take the position that Respondents have not shown by clear and convincing evidence that the `338 patent is invalid.

In order to prove obviousness, it must be demonstrated by clear and convincing evidence that the invention of claim 27 would have been obvious in light of the combined teachings of items of prior art relied on by Respondents. See Graham v. John Deere, 383 U.S. at 37; Jones, 727 F.2d 1524, 1530-32 (Fed. Cir. 1984); Litton, 97 F.3d at 1566 (section 103 obviousness analysis requires a determination of the scope and content of the prior art, the differences between the prior art references and the claimed invention and the secondary indicia of nonobviousness). In addition, it must be shown that

[75] Section 103 of the Patent Act is quoted above in the portion of this section addressing the `752 patent.

one of ordinary skill would have known to combine these items. See Uniroyal, 837 F.2d at 1050-1051.[76] As discussed below, the requisite showing has not been made to find claim 27 of the '338 patent obvious in view of the prior art.

Neither the Torelli Article, nor the SGS data books, nor SGS technical notes include any disclosure or teaching relating to the concept of permanently inhibiting the programming of verified cells, an essential function of claim 27. FF IV 175-189. Furthermore, Samsung introduced no evidence at trial to show that the permanent inhibition of programming of verified cells would have been obvious to an individual of ordinary skill. FF IV 191. Nor did Samsung offer any testimony to suggest that one would know to combine the cited prior art. FF IV 192.

In fact, Samsung has argued against obviousness by taking the position that the function of permanently inhibiting the programming of correctly verified cells would be irrelevant or meaningless to the operation of binary devices. Thus, Samsung has conceded that an individual of ordinary skill would not recognize the possibility that the endurance and operation of a binary EEprom device could be improved by terminating the programming of correctly verified cells. See also FF IV 198, 199.

There is nothing in the prior art relied on by Samsung to indicate that the programming of a cell should be stopped or terminated upon verification. FF IV 175-189. In fact, the Torelli Article, SGS data books and SGS technical notes suggest the opposite. These documents suggest that all the cells being programmed should be verified after each programming pulse. At most, they

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[76] An individual of ordinary skill in the art of flash memory has at least a bachelor's degree in a field such as electrical or computer engineering (or experience equivalent thereto) and at least a few years of work experience with EEproms. FF IV 167-172.

teach that the inhibition of further programming pulses is a conditional event that must occur on a pulse-by-pulse basis. FF IV 155-158. Thus, if the "read" conditions on any given cell changes after a cell has been "verified" (i.e., the device correctly or incorrectly reads that the cell is no longer in the "written" state), the respective disclosed devices apply an additional programming pulse(s) to the previously verified cell. FF IV 154, 100. Such a result is contrary to the requirement of claim 27 that the programming of a verified cell be inhibited or disabled until all the addressed cells have been verified.

Furthermore, it was undisputed at trial that the concept of "permanently inhibiting" or "terminating" the programming of verified cells was not obvious to an individual of ordinary skill in 1989. See FF IV 198-226. The non-obviousness of the permanent inhibit feature is demonstrated by the fact that Toshiba, the original designer of the NAND architecture, did not include a permanent inhibit feature in its original 4Mbit flash memory product despite the fact that it is beneficial to the NAND device. FF IV 199, 226.

Consequently, none of the prior art cited by Samsung can individually or in combination invalidate claim 27 of the `338 patent.

The validity of the `338 patent, including claim 27, is further supported by secondary indicia of validity. The `338 patent has been and will be crucial to SanDisk's success in the mass storage flash memory market. FF IV 200. As of 1994, SanDisk was the worldwide leader in the mass storage flash memory with approximately a 40% market share. FF IV 203. Furthermore, Intel, the world's largest commodity flash memory producer, has entered into a licensing agreement for all of SanDisk's patents, including the `752 and `338 patents. FF IV 201.

The Administrative Law Judge finds that it has not been shown by clear and convincing evidence that claim 27 of the `338 patent is invalid due to obviousness.

V. INFRINGEMENT

A. General Law of Infringement

To establish literal infringement, every limitation set forth in a claim must be found in an accused product, exactly. Southwall Technologies, Inc. v. Cardinal IG Co., 54 F.3d 1570, 1575 (Fed. Cir. 1995). Accord Graver Tank & Mfg. Co. v. Linde Co., 339 U.S. 605, 607 (1950)(Literal infringement of the asserted claim occurs "[i]f accused matter falls clearly within the asserted claim ....").

In the case of a means-plus-function claim, to determine whether a claim is met literally, one "must compare the accused structure with the disclosed structure, and must find equivalent structure as well as identity of claimed function for that structure." Pennwalt Corp. v. Durand-Wayland, Inc., 833 F.2d 931, 934 (Fed. Cir. 1987)(en banc)(emphasis in original), cert. denied, 485 U.S. 1009 (1988).[77]

Limiting patent enforcement exclusively to literal infringement "would place the inventor at the mercy of verbalism and would be subordinating substance to form." Graver Tank, 339 F.2d at 607. Thus, if the accused product or process does not literally infringe the patent at issue, it may infringe under the doctrine of equivalents. See In re Certain Doxorubicin and

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[77] "Equivalence" under a means-plus-function analysis should not be confused with "equivalence" under the doctrine of equivalents (discussed herein below). "In the context of section 112 ... an equivalent results from an insubstantial change which adds nothing of significance to the structure, material, or acts disclosed in the patent specification." Valmont, 983 F.2d at 1043. A determination of section 112 equivalence does not involve the tripartite function-way-result test of the doctrine of equivalents. Id. The "sole question is whether the single means in the accused device that performs the stated function is an equivalent of the corresponding structure described in the specification as performing that function." Intel Corp., 946 F.2d at 842; D.M.I., Inc. v. Deere & Co., 755 F.2d 1570, 1575 (Fed. Cir. 1985). There is no equivalent "function" under section 112; only equivalent means. Valmont, 983 F.2d at 1043.

Preparations Containing Same, 20 U.S.P.Q.2d 1602, 1608 (United States Int'l Trade Comm'n 1991)("An allegation of infringement under the doctrine of equivalents presumes that literal infringement does not exist, i.e., that the asserted patent claims, properly interpreted, do not in terms cover the accused device or process.").

In Hilton-Davis Chem. Co. v. Warner-Jenkins Co., Inc., 62 F.3d 1512 (Fed. Cir. 1995)(per curiam), the Court of Appeals for the Federal Circuit held that the doctrine of equivalents "applies if, and only if, the differences between the claimed and accused products or processes are insubstantial."[78] 62 F.3d at 1517 (citing Graver Tank, 339 U.S. at 610). An insubstantial change is one "which, from the perspective of one of ordinary skill in the art, adds nothing of significance to the claimed invention." Valmont, 983 F.2d at 1043. "[T]he vantage point of one of ordinary skill in the relevant art provides the perspective for assessing the substantiality of the differences." Hilton-Davis, 62 F.3d at 1519 (citing Valmont, 983 F.2d at 1043).

In Hilton Davis, the court stated that "[i]n applying the doctrine of equivalents, it is often enough to assess whether the claimed and accused products or processes include substantially the same function, way and result." 62 F.3d at 1518. In many cases, the substantiality of the differences between the claimed and accused products or processes have been measured by reliance on the "so-called triple identity, or function-way-result, test ...." Yet, the court held that "[i]t goes too far, however, to describe the function-way-result test as `the' test for

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[78] The Federal Circuit has held similarly in other cases. See, e.g., London v. Carson, Pirie, Scott & Co., 946 F.2d 1524, 1538 (Fed. Cir. 1991); Perkin-Elmer Corp. v. Westinghouse Elec. Corp., 822 F.2d 1528, 1535 (Fed. Cir. 1987).

equivalency announced by Graver Tank." Id. at 1518. An "important factor" to be considered in making the equivalence determination is "whether persons reasonably skilled in the art would have known of the interchangeability of an ingredient not contained in the patent with one that was." Id. at 1519 (quoting Graver Tank, 339 U.S. at 609).

In order to establish infringement under the doctrine of equivalents, one must demonstrate that the equivalent of each claim limitation is present. Laitram Corp. v. Rexnord, Inc., 939 F.2d 1533, 1535 (Fed. Cir. 1991); Pennwalt, 833 F.2d at 935-36.[79]

A patentee may be estopped from asserting a claim in a particular manner due to prosecution history estoppel. The Federal Circuit has explained that "the essence of prosecution history estoppel is that a patentee should not be able to obtain, through the doctrine of equivalents, coverage of subject matter that was relinquished during prosecution to procure issuance of the patent." Hoganas AB v. Dresser Indus., Inc., 9 F.3d 948, 951-52 (Fed. Cir. 1994).[80] Accord Sofanor Danek Group, Inc. v. Depuy-Motech, Inc., 74 F.3d 1216, 1222 (Fed. Cir. 1996)(citing Exhibit Supply Co. v. Ace Patents Corp., 315

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[79] With respect to the doctrine of equivalents, the Federal Circuit has held that:

> [A] patentee must still provide particularized testimony and linking argument as to the `insubstantiality of the differences' between the claimed invention and the accused device or process, or with respect to function, way, result test when such evidence is presented to support a finding of infringement under the doctrine of equivalents. Such evidence must be presented on a limitation-by-limitation basis.

Texas Instruments, Inc. v. Cypress Semiconductor Corp., 90 F.3d 1558, 1567 (Fed. Cir. 1996).

[80] Whether one should apply prosecution history estoppel is a question of law. Southwall Technologies, 54 F.3d at 1579; Hoganas, 9 F.3d at 952.

U.S. 126, 136 (1942)).

"Similarly a patentee may not assert a range of equivalents that captures art already in the public domain." Sofanor, 74 F.3d at 1222 (citing Wilson Sporting Goods Co. v. David Geoffry & Assocs., 904 F.2d 677, 683 (Fed. Cir.), cert. denied, 498 U.S. 992 (1990)).

"Infringement, whether literal or under the doctrine of equivalents, is a question of fact." Hilton-Davis, 62 F.3d at 1520 (citing, inter alia, Winans v. Denmead, 56 U.S. (15 How.) 330, 338 (1854)); Graver Tank, 339 U.S. at 609-10.

A party alleging infringement has the burden of proving infringement by a preponderance of the evidence. Envirotech Corp. v. Al George, Inc., 730 F.2d 753, 758 (Fed. Cir. 1984); Hughes Aircraft Co. v. United States, 717 F.2d 1351, 1361 (Fed. Cir. 1983).

B. Claims 1, 2 and 4 of the `752 Patent Are Infringed

Complainant SanDisk adduced evidence during the hearing concerning infringement of the `752 patent by the following Samsung devices: 16 Mbit (original and first generation after design change), 32 Mbit (original), and 64 Mbit (original).[81] In this investigation, those devices have often been referred to as having Samsung's "original designs." For the purposes of the infringement analysis under the `752 patent those devices are also referred to in this Initial Determination as having Samsung's "original designs."[82]

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[81] SanDisk does not maintain that Samsung's 4 Mbit devices infringe the `752 patent. FF V 2.

[82] Additionally, Samsung adduced evidence at the hearing concerning the following Samsung devices: 16 Mbit (after design change), 32 Mbit (after design change) and 64 Mbit (after design change). These devices are referred to as having Samsung's "new designs." See, e.g., Pathak, Tr. 693. They are (continued...)

1. Samsung's Original Designs

At the hearing, Samsung's infringement expert, Mr. Thomas, did not offer any opinion as to whether Samsung's flash memory circuits with the original designs infringe the `752 patent. FF V 22. However, SanDisk adduced more than a preponderance of evidence that Samsung's original design devices literally infringe claims 1, 2 and 4 of the `752 patent.[83]

a. Claim 1 of the `752 Patent

The evidence offered at the hearing establishes that Samsung's flash memory devices with the original designs possess each of the limitations contained in the first element recited in claim 1.

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[C]

] FF V 23-30.

The evidence further establishes that Samsung's flash devices (original design) possess a "means for selecting a plurality of sectors" and an "individual register" as provided for in the patent.

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[82](...continued)
discussed further below.

[83] In the alternative, any differences that exist between Samsung's devices with the original designs and the literal scope of the claims are insubstantial, and thus Respondents infringe under the doctrine of equivalents.

] FF V 31-39.

Finally, the evidence shows that Samsung's flash devices (original design) possess a "means for simultaneously performing the erase operation on only the plurality of selected sectors." [

[C]

] FF V 40-41.

Because Samsung's devices with the original designs possess each element of claim 1 of the `752 patent, the Administrative Law Judge finds that the devices literally infringe claim 1 of the `752 patent. While not disputing that certain original design Samsung flash memory products are capable of performing multisector erase, Samsung and OUII take the position that none of the Samsung devices is infringing because Samsung does not sell them with a controller. However, as discussed above, a controller is not part of the

invention claimed in the `752 patent.[85]

Another issue has been raised with respect to Samsung's 16 Mbit devices. There have been two generations of 16 Mbit devices after a design change in which Samsung allegedly attempted to remove the multisector erase from its products. The first generation after design change, as mentioned above, has been referred to as having a so-called "original design." Nevertheless, Samsung argues that it cannot infringe the asserted claims of the `752 patent because of the allegedly successful removal of the multisector erase capability.

However, the record evidence demonstrates that Samsung's first generation 16 Mbit devices (after design change) are capable of performing multisector erase. [

[C]

] FF V 49-60. The new sequence was discerned by Complainant's expert, Mr. Pathak, and was often referred to during the hearing as the "Pathak sequence."

It is uncontroverted that the Pathak sequence actually works to perform multisector erase. Samsung's expert conceded, as follows:

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[85] Although Samsung's circuits do not possess a controller, they have few uses without a controller. FF V 43. Indeed, the evidence shows that Samsung's devices are often sold with a controller, and that customers use Samsung's devices with a controller. FF V 42, 82. A TDK flash memory card using Samsung flash memory chips with a controller was admitted into evidence. FF V 82. In addition, at least one Samsung customer, M-Systems, not only used the multisector erase feature in its products, but complained to Samsung about its decision to remove the feature. FF V 14-15. Therefore, if a controller were required in order to practice the claimed invention, there is strong evidence that Samsung would be considered a contributory infringer and/or to have induced infringement under 35 U.S.C. § 271(b)-(c).

[BY COMPLAINANT'S COUNSEL]

Q. [T]he 16-meg first generation after-design change, as I understand your testimony, that product is capable of performing multi-block erase under the Pathak sequence; is that right?

A. That's true. I already testified to that effect, Your Honor.

Q. And it's accurate, isn't it, that assuming that sequence works, which you testified to, that product satisfies the element means for selecting in claim 1 of the '752 patent?

A. But that's not a sequence which is -- it's a contrived sequence which is out of the scope of the device data book of the way devices are supposed to be operated, Your Honor.

Q. I understand that, but in the realm in which that sequence operates, it satisfies the element means for selecting a plurality of sectors.

A. It does select a plurality of sectors using the Pathak sequence.

Q. And the structure of that device has an individual register associated with each sector, right? That's device number 5.

A. Yes.

Thomas, Tr. 1601-1602.

Samsung argues that the Pathak sequence is contrived and not within the parameters of its data book. However, nothing would prevent Samsung from releasing a data book which sets forth the Pathak sequence. See Thomas, Tr. 1552-1553.

Samsung also argues that because of the rapid timing required to utilize the Pathak sequence Samsung would not guarantee to their customers that the sequence would work, and further that commercial controllers are not available that work fast enough. However, there is evidence that commercial controllers are in fact capable of operating fast enough to implement the Pathak sequence.

FF V 65.

Moreover, the fact remains that the Pathak sequence has been demonstrated to implement multisector erase in the accused device. Because Samsung's devices are capable of performing multisector erase, they are infringing regardless of whether Samsung's customers actually use the multisector erase feature. See Intel Corp., 946 F.2d at 832 (holding that "the accused device, to be infringing, need only be capable of operating in the [infringing] mode.").[86]

Consequently, Samsung's first generation after designs change 16 Mbit devices are capable of performing multisector erase, see FF 61-62, and literally infringe claim 1 of the `752 patent along with the other Samsung devices containing the "original designs."

b. Claim 2 of the `752 Patent

Samsung original design devices also infringe claim 2 of the `752 patent. [

[C]

] FF V 34.

[[C]

] FF V 48.

These features literally satisfy claim 2 of the `752 patent which provides

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[86] Unlike the device in High-Tech Medical Instrumentation, Inc. v. New Image Indus., Inc., 49 F.3d 1551 (Fed. Cir. 1995), a case relied on by Respondents, in which infringement occurred only if screws used to secure a camera to its housing were removed or loosened, the Samsung devices do not require alteration in order to operate in an infringing manner. The circumstances in this case are in fact similar to those in the Intel case in which the device, "although not specifically designed or sold to operate in that [infringing] manner, could be programmed to do so ...." Id. at 1555-56 (discussing the Intel case).

that "the simultaneously erasing means is responsive to the status in each of the individual registers, such that only the selected sectors are included in the erasing." See FF V 44.

c. Claim 4 of the `752 Patent

Samsung's devices (original design) also infringe claim 4 of the `752 patent. FF V 45. [

[C]

] FF V 47. These features literally satisfy claim 4 of the `752 patent which provides that "all the individual registers are simultaneously resettable to a status indicating the associated sectors as not selected."

2. Samsung's New Designs

The Administrative Law Judge declines to make a determination as to whether devices with Samsung's new designs (i.e., Samsung's 16 Mbit (second generation after design change), 32 Mbit (after design change) and 64 Mbit (after design change)) infringe the claims of the `752 patent.

As a threshold matter, Samsung has not provided any documentary evidence that it is importing products with the new designs which have allegedly been redesigned to remove the multisector erase feature. FF II 4-6. [

[C]

] FF II 3, 5.

Furthermore, documentation produced by Samsung is insufficient to make a definitive determination regarding whether Samsung's new designs are capable

of performing multisector erase operations. FF V 92, 94. The inaccuracies, inconsistent signal names and unexplained symbols make it impossible to have confidence in any analysis regarding possible infringement by these products. FF V 93, 95-98, 101-102.

As demonstrated by the testimony of Complainant's witness, Mr. Pathak, determining whether the complex circuits for Samsung's flash devices contain an undisclosed command sequence for performing multisector erase requires access to either: (1) internal signal lists and internal signal timing diagrams, or (2) the complete schematics on the computer data base. FF V 83, 85-87, 92, 104. Mr. Pathak was provided with neither form of documentation. FF V 88, 96.

The schematics produced by Samsung were merely "cut and paste" documents from the actual computer data base. FF V 96. These documents do not fully and completely reflect the operation of Samsung's new designs. Even an experienced Samsung design engineer admitted that sometimes one must refer to the computer data base to understand the operation of a device. FF V 103. In fact, Samsung's own expert testified that a thorough analysis of a Samsung flash memory circuit would take an individual person years to accomplish. FF V 84. SanDisk and its expert cannot be expected to have performed an infringement analysis on Samsung's new designs with the documentation they were provided.

The position of Samsung and OUII that SanDisk's expert, Mr. Pathak, had sufficient documentation to make a definitive determination regarding whether Samsung new designs possess an undisclosed command and timing sequence for performing the claimed multisector (multiblock) erase function is erroneous. FF V 85, 92-94. There is a significant difference between the documentation necessary to simulate (or, even build) a Samsung NAND flash memory device and

the type of information necessary to understand the full capabilities of the device during an erase operation. See FF V 85, 92-94, 103, 104-116.

The internal signal list and timing diagrams that SanDisk's expert had for Samsung's original designs are precisely the type of documents that are necessary to understand the full capabilities of the complex Samsung flash memory devices. FF V 88-95. By reviewing these internal signal documents, Mr. Pathak was able to understand the interaction of all the relevant circuits and discover a hidden "back door" for performing multiblock erase that was not disclosed in the Samsung data books. See FF V 112. Without such documentation, the "Pathak Sequence" would never had been uncovered. FF V 83-85, 87, 102.

Samsung did not produce to SanDisk internal signal documentation for its new designs (or access to the only known substitute, its computer data base). Thus, SanDisk was deprived of the opportunity to make any definitive determination regarding whether Samsung's new designs also possess a "hidden" command sequence for performing the multisector erase operation claimed in the `752 patent. Id.

Consequently, Complainant SanDisk did not have an adequate opportunity to test through discovery whether Samsung's devices with the new designs are capable of infringement. Furthermore, [

[C]

] Therefore, they are not part of this investigation, and no determination is made with respect to whether they would infringe the claims at issue of the `752 patent.

C. **Claim 27 of the `338 Patent Is Infringed**

Complainant SanDisk takes the position that Samsung's devices practice each of the elements of claim 27, including the seven disputed elements covered in the section of this Initial Determination on claim construction, and that therefore Samsung infringes claim 27 literally or, in the alternative, under the doctrine of equivalents.

The Samsung respondents take the position that their devices do not practice at least six of the disputed claim elements, and that therefore their devices do not infringe claim 27 either literally or under the doctrine of equivalents. Respondents' Post-Hearing Br. at 17.

OUII takes that position that the Samsung devices do not practice all of the disputed elements of claim 27, and that therefore the devices are not infringing.

Samsung's Flash EEprom products are binary devices. As discussed above in the section on claim construction, although the preferred embodiment of the `338 patent is a multi-state device, the specification states that the claimed invention may be applied to a binary device. Indeed, claim 27 reads on a binary device. However, Samsung argues that because of prosecution history estoppel, a binary device cannot be found to infringe claim 27. SanDisk and OUII oppose Samsung on this point.

Before examining each of the individual elements of claim 27, the question of prosecution history estoppel is addressed as a threshold matter.

Samsung argues that during the prosecution of the `338 patent, SanDisk distinguished claim 27 over U.S. Patent No. 4,460,982 to Gee et al. on the basis that the `982 Gee patent would work only for binary memory cells, not multistate cells covered by the `338 patent, and further that SanDisk is estopped from now asserting that binary devices infringe the asserted claims

under the doctrine of equivalents.

In order to distinguish claim 27 of the `338 patent over the prior art, particularly Gee et al., the applicants' agent represented, as follows:

> Claim 27-28 has [sic] been amended to recite inhibiting of further programming of correctly verified cells rather than selective programming of unverified cells.
>
> Gee et al. disclose a programming system operating in parallel on 8 bits of addressed cells. If bits 2, 5 and 7 are to be programmed to the "0" state, programming pulses will be applied to all three cells as long as one of these cells are not verified correctly. This scheme does not work for memory cells having more than two states since some cells will reached [sic] their desired state earlier than others and will continue to pass [sic] the desired state if not stopped.
>
> Thus, Giebel and Gee et al., individually or in combination do not teach or suggest a programming system with means for inhibiting further programming of correctly verified cells among the plurality of addressed cells. It is believed amended claims 27-28 along with amended claim 33 are allowable.

CX 8 (`338 Prosecution History) at SD008951 (emphasis added).

The statements quoted above, and relied on by Respondents (see RPFF 373), say nothing about binary devices. The applicants, through their agent, indicated to the Examiner that their invention, as claimed in claims 27-28 and 33, is suitable for multistate devices because of its ability to inhibit further programming of correctly verified cells, whereas Gee et al. is unsuitable for multistate devices. However, the statements made to the Examiner do not preclude the claim from covering binary devices. These statements pointing out the advantages of the claimed invention with respect to multistate devices do not indicate that the claimed invention and that of Gee et al. operate in the same manner with respect to binary devices. Indeed, the inhibiting of further programming of verified cells occurs regardless of whether the invention of claim 27 is used in a binary device or a multistate

device. As discussed above in connection with claim construction, it is also useful to prevent unnecessary programming in both binary and multistate devices.

Therefore, the Administrative Law Judge finds that prosecution history estoppel does not apply in the case of the `338 patent to prevent claim 27 from covering binary devices such as Samsung's flash EEprom products.

Consequently, Samsung's devices and the disputed elements of claim 27 of the `338 patent are discussed below. For the purposes of this infringement analysis, all of Samsung's products are addressed together.[87] See FF V 119, 136.

1. **Erase Electrode Element**

[[C]]in Samsung's flash memory devices constitutes an erase electrode as that term is used in claim 27 of the `338 patent. See FF V 123. As noted above, "erase electrode" is properly defined in the context of claim 27 as a terminal to which erase voltage conditions are applied to draw electrons off the floating gate. See, supra, at 51. [

[C]

] FF V 125-131. This functionality squarely falls within the properly interpreted scope of the term "erase electrode."

Samsung attempts to avoid a finding of infringement by reading

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[87] The Samsung devices are not addressed as having "old" or "new" designs for the purposes of an infringement analysis under claim 27 of the `338 patent. Samsung's redesign was directed at the multi-block erase feature of its devices, which is not the subject matter of the `338 patent.

additional limitations into this element (e.g., that there must be a separate erase electrode for each cell, or that it must be "physically distinct" from any other structure in the device). However, there is no language in the patent or the file history that would require the imposition of these limitations or otherwise vary the ordinary meaning of the term. Thus, the erase electrode limitation must be properly interpreted (as both SanDisk and OUII have argued) in accordance with its ordinary meaning and without Samsung's additional proposed limitations. Applying this interpretation, Samsung's flash memory devices clearly satisfy the "erase electrode" element.

The Administrative Law Judge finds that given its proper interpretation, the term "erase electrode" is broad enough to encompass Samsung's devices under the standards of literal infringement. However, SanDisk and Samsung have raised the issue of the doctrine of equivalents with respect to this claim element.

As an alternative to literal infringement, Samsung's devices would satisfy this claim limitation under the doctrine of equivalents. Samsung argues that its devices do not satisfy this element under the doctrine of equivalents because there are differences between [[C]] and the erase gate disclosed in the preferred embodiment. See, e.g., Respondents' Post-Hearing Br. at 22.

The relevant inquiry under the doctrine of equivalents is not merely whether there are structural differences between the accused devices and the preferred embodiment, but whether the differences between the claimed erase electrode and the Samsung structure are substantial (e.g., whether one of ordinary skill would have known of the interchangeability of [[C]] and the erase electrode of the preferred embodiment). See Hilton-Davis, 62 F.3d at 1519.

Samsung has not argued that one of ordinary skill would lack knowledge of the interchangeability between [[C]] and a dedicated erase gate. In fact, the record establishes that other companies have used [[C]] instead of an erase gate as the terminal to which erase voltage conditions are applied to draw electrons off the floating gate during the erase operation. See FF III 44; CPFF 265-271; SPFF 102.

Indeed, [[C]] performs the same function (acting as a terminal for receiving erase voltage) in substantially the same way (creating a potential difference between [[C]] and the control gate) which pulls electrons off the floating gate to obtain the same result (removal of electrons form the floating gate) as the erase electrode referenced in claim 27. FF V 126-131.

Accordingly, if the erase electrode element is not literally satisfied by the [[C]] it is met under the doctrine of equivalents.

2. **Increment/Decrement Element**

[

[C]

] FF V 134-135. This feature alone satisfies the requirement of claim 27 that "a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions." See, supra, at 53-57. [

[C]] FF V 136.

Samsung argues that its devices do not satisfy the increment/decrement element of claim 27 because [

[C]

] See Choi, Tr. 1351-1352. Moreover, Samsung's asserted claim construction, requiring that both erase and programming operations be effected by successive applications of voltage, was rejected above.

Accordingly, it is found that Samsung's devices practice this element of claim 27.

3. Temporary Storage Means

As discussed above, the element "means for temporarily storing a chunk of data for programming a plurality of addressed cells" requires data to be stored in a latch or equivalent structure at least until the cell is verified and programming to the cell is inhibited. [

[C]

] FF V 141-144. Accordingly, Samsung's devices fall within the properly interpreted scope of this element.

Samsung's argument that its devices lack this claim element is based on an incorrect interpretation of the relevant claim language. In particular, Samsung contends that this element must be construed to require data to be stored "during the entire programming process." Respondents' Post-Hearing Br. at 22. That proposed construction of the claim was rejected above.

Samsung also argues that its devices [[C]

] Respondents' Post-Hearing Br. at 23.

However, this argument is contradicted by Samsung's own technical documentation. [

[C]

] Id.

Although the terminology is somewhat different, the function carried out in Samsung's devices is the exact same function performed by the temporarily stored data in the `338 patent. See FF V 144; CX 2 (`338 Patent) at col. 19, line 42 through col. 20, line 16. Accordingly, Samsung's devices satisfy this means-plus-function element.[88]

4. Parallel Programming Means

Both SanDisk's infringement expert and Samsung's infringement expert agree that Samsung's flash memory devices perform the function of programming

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[88] [

[C]

] Respondents' Post-Hearing Br. at 23. As set forth above, these alleged differences do not place the Samsung devices outside the scope of this claim element. Aside from these "differences," [

[C]], and satisfy the second prong of a "means-plus-function" analysis. FF V 142-144.

in parallel into the addressed cells.[89] FF V 145-146.

Nevertheless, Samsung contends that its devices do not satisfy this element because they do not perform the programming function in the same manner as the Hot Electron Injection programming method described in the preferred embodiment of the `338 patent. However, as explained above, claim 27 contains no limitation as to the manner or method of programming. Indeed, from the perspective of the patented invention, there is no difference between programming using Fowler-Nordheim tunneling and programming using Hot Electron Injection inasmuch as both force electrons through the oxide onto the floating gate, which is all that is needed to program a flash memory.

Accordingly, it is found that Samsung's devices practice this claim element.

5. Verifying Means

Samsung's flash memory devices perform the function of "verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data." See FF V 152. [

[C]

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[89] Samsung's devices do not have a source mux or drain mux as shown in Figure 14 of the `338 patent. FF V 148. However, because Samsung uses a NAND architecture, the functions of the muxes can be performed without using these structures. It is logical not to use such muxes in the Samsung designs. FF V 149-151. The logical elimination of these unnecessary structures does not affect the infringement analysis with respect to this means-plus-function claim element. See Data Line Corp. v. Micro Technologies, Inc., 813 F.2d 1196, 1202 (Fed. Cir. 1987) ("We conclude that a reasonable jury could have found that a single sensor with multiplex switching is the equivalent of multiple sensors with multiple switches, and that these are within the scope of the limitation `means for sensing' in claim 1.").

] FF V 154.

The arguments by Samsung and OUII that Samsung's devices lack the claimed verifying means are based on a flawed interpretation of the relevant claim language. It is argued that the Samsung devices do not perform the function of "verifying the programmed data ... with the chunk of stored data" because [[C]

] See SPFF 305; RPFF 458. However, the `338 patent does not require verification of cells that are targeted to be in the erased state. Indeed, as detailed above, the `338 patent expressly states in the context of discussing the verification function that "if each memory cell is to store K states, then at least K - 1, or preferably K reference levels need be provided." CX 2 at col. 11, lines 56-58. In other words, in the case of a two state device, only a single reference level need be used for performing the verification function (i.e., where "0" equals the programmed state, the device only needs to determine whether the cell has reached the "0" state, and can ignore cells targeted to remain in the erased state). The `344 patent (which is incorporated by reference into the `338 patent) similarly discloses that a single sense amplifier and a single reference level can be used to differentiate between conduction states "1" (or erased) and "0" (or programmed).

As discussed above, before a flash EEprom sector can be programmed, it must be erased. See FF V 158. As a result, all of the cells in the sector are necessarily in the erased state at the beginning of the programming process. In a binary implementation of the `338 patent, cells targeted to be in the erased state are then automatically inhibited from programming before

the first pulse is applied. FF III 68.[90] Thus, it would be obvious to anyone of ordinary skill in the art that there is no reason to verify repeatedly whether cells targeted to be in the erased state are in fact in the erased state, since absent a device failure, there is no way for such cells to come out of the erased state that they were in at the beginning of the programming cycle.[91] FF III 71; Pathak, Tr. 823-831; Mehrotra, Tr. 342-351.

Accordingly, the evidence shows that Samsung's devices perform the "verify" function recited in the `338 patent.[92]

Both Samsung and OUII argue that Samsung's devices do not satisfy the "means for verifying" element either literally or under the doctrine of

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[90] Samsung has proposed a finding that: "Cells in the `338 patent that are to remain in the erase state never encounter programming conditions, and, therefore, there is no need to make a change in their programming conditions." See RPFF 479 (citing Harari, Tr. at 266).

[91] Indeed, at the hearing, Samsung's expert Dr. Allen testified that the M293, a device alleged to invalidate the `338 patent, "does meet the language of the claim in `338," even though that device performed a verify operation "just in the case of going from zero to one." (i.e., only for cells targeted to be in the programmed state). Allen, Tr. 1179-1180; see also Gross, Tr. 1447-1452; CX 204 (concerning the fact that M293 only verifies cells targeted to be in the programmed state, and performs no verification on cells targeted to remain in the erased state). The same type of verification is performed by the Samsung devices. FF V 152-157.

[92] Samsung also argues that it does not verify the programmed data with the chunk of stored data because it does not store "program data," and there is "no temporary storage of data for programming." Respondents' Post-Hearing Br. at 25. As set forth previously in connection with the temporary storage means, the differences between the Samsung devices and the `338 patent with respect to the storage of "program data" are largely semantic, while in other instances Samsung has in fact referred to the stored information as "program data." See CX 56. [

[C]

] See FF V 135, 153-154. This is precisely what is claimed in the `338 patent.

equivalents, because their circuitry is not equivalent to that described in the `338 patent.

As noted above, the `338 patent specifically contemplates a binary device in which a single reference level is used. See SPFF 133-134; CPFF 775. A person of ordinary skill seeking to implement Figure 11-E in a binary device with a single reference level (as is disclosed in the `344 patent at col. 11, lines 56-58) would only use a single sense amplifier to perform that function. See FF III 71-72. Moreover, in its discussion of Figure 11-E, the `344 patent specifically acknowledges that for a four-state device, "only three sense amplifiers and three reference levels are required to sense the correct one of four states," and that a single sense amp and a single reference level can be used to "differentiate correctly between conduction states '1' and '0'." FF V 163; CX 3 (`344 Patent) at col. 26, lines 51-60. Thus, the `344 patent explicitly teaches that for a binary device, only one sense amplifier and one reference level is required to sense the correct state. Finally, the `344 patent specifically discusses an embodiment of Figure 11-E in which "a single sense amplifier" is used. FF V 164; CX 3 at col. 26, lines 8-15. These disclosures are more than adequate to support the conclusion that Figure 11-E would be reduced to a single sense amplifier in a binary device, and that such a structure is the structural equivalent of Figure 11-E.[93]

[

[C]

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[93] The testimony of Samsung's expert, Dr. Allen, also supports this interpretation. Dr. Allen testified that one of ordinary skill in the art would use a single sense amplifier to verify the programming of a binary device. Dr. Allen further testified that the M293, which uses a single sense amplifier (and no comparator circuit) to perform the verify operation, satisfies the "means for verifying" element of claim 27. Allen, Tr. 1173-1180; see also FF III 71, IV 136.

[C]

] FF V 154. As set forth above, this structure is identical to, or at the very least the structural equivalent of, the structures disclosed in the `338 patent for binary simplifications of Figure 11-E. FF V 155-157. Accordingly, Samsung's devices satisfy this element as properly construed.

6. Inhibiting Means

Samsung uses [[C]]to perform the function of "inhibiting further programming of correctly verified cells among the plurality of addressed cells." The latch used by Samsung is equivalent to latch 721 in Figure 16 of the `338 patent. See FF V 166-171.

Samsung argues that it does not practice this element because it performs the claimed function in a different manner than the preferred embodiment in the patent. This claim element is written in means-plus-function form. The law provides that if an accused device employs a structure that is identical or equivalent to that disclosed in the specification in order to perform the identical function required in the claim, then infringement will be found. Valmont, 983 F.2d at 1042.[94] Claim 27 contains no limitation concerning the manner in which a covered structure is to operate, and Samsung has provided no legal basis upon which to find that infringement may be avoided because of the manner in which the structure operates.

Indeed, Samsung's devices perform the function of inhibiting further

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[94] See also Intel Corp., 946 F.2d at 842; D.M.I., Inc. v. Deere & Co., 755 F.2d 1570, 1575 (Fed. Cir. 1985).

programming of a correctly verified cell, until all cells in the chunk have been verified. Pathak, Tr. 840-846; SPFF 312. As in the `338 patent, the inhibiting function is accomplished in Samsung's products [

[C]

] SPFF 313.

[

[C]

] Thomas, Tr. 1119-1120; SPFF 315. In contrast, flipping the latch 721 disclosed in the `338 patent causes 0 volts to be applied to the drain of the disclosed NOR cell. FF V 177; SPFF 316 Nevertheless, no additional structure is required with respect to the latch 721 in order to accomplish the inhibiting function claimed in the `338 patent. Samsung's products therefore include the inhibiting means recited in claim 27.

7. Final Means-Plus-Function Element

In denying that it practices the final element of claim 27, Samsung's only argument is that this final element incorporates three previous elements (parallel programming means, means for verifying, and means for inhibiting further programming) that Samsung contends are not present in its devices. Respondents' Post-Hearing Br. at 27-28. Inasmuch as Samsung practices those three claim elements, Samsung also practices this final claim element. See FF V 179-183.

Conclusion

Based on the foregoing analysis of Samsung's devices, the Administrative Law Judge finds that Samsung infringes claim 27 of the `338 patent literally, or in the alternative, under the doctrine of equivalents.

VI. DOMESTIC INDUSTRY

A. Economic Requirements

Section 337(a)(1)(B), which is asserted against Respondents in this investigation, applies "only if an industry in the United States, relating to the articles protected by the patent. . . exists or is in the process of being established." 19 U.S.C. § 1337(a)(2).

The requisite domestic industry is defined in section 337 as follows:

> (3) For purposes of paragraph (2), an industry in the United States shall be considered to exist if there is in the United States, with respect to the articles protected by the patent . . . concerned --
>
> (A) significant investment in plant and equipment;
>
> (B) significant employment of labor or capital; or
>
> (C) substantial investment in its exploitation, including engineering, research and development, or licensing.

19 U.S.C. § 1337(a)(3).

The domestic industry requirement is satisfied by meeting the criteria of any one of the three factors listed above. Certain Concealed Cabinet Hinges and Mounting Plates, Inv. No. 337-TA-289, Comm'n Op. at 19-20 (1990). Complainant bears the burden of establishing that the domestic industry requirement is satisfied. Id. at 22.

During the course of hearing, Respondents conceded that Complainant SanDisk's domestic activities satisfy the economic prong of the domestic industry requirement. Tr. 657-659. Furthermore, the record evidence establishes that SanDisk's activities and investments establish a domestic industry under all three of the factors enumerated in the statute. FF VI 2-21.

B. Technical Requirements

The `752 Patent

In order to satisfy the domestic industry requirement with respect to the `752 patent, SanDisk asserts that it practices claims 1, 2 and 4.[95] As discussed in detail below, all of SanDisk's products embody claims 1, 2 and 4 of the `752 patent. See FF VI 22. In fact, the `752 patent is based on the SanDisk inventors' work in developing SanDisk's first flash memory products. FF V 123.

Claim 1

"One or More Integrated Circuit Chips ..."

[[C]

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[95] With respect to both the `752 patent and the `338 patent, Complainant SanDisk takes the position that it practices the same claims that it asserts against Respondents. Although it is found herein that SanDisk does in fact practice the claims asserted against Respondents, such a correspondence of claims is not required in order to demonstrate that the domestic industry requirement is satisfied.

In Certain Microsphere Adhesives, Process for Making Same, and Products Containing Same Including Self-Stick Repositionable Notes, Inv. No. 337-TA-366, USITC Pub. 2949 (Jan. 1996), the Commission stated upon reviewing the pertinent portions of the statute that "important questions in section 337 investigations are whether there is significant or substantial commercial exploitation, and whether the complainant is exploiting or practicing the patent in controversy." Comm'n Op. at 8. The Commission held, however, that "[o]ur review of the pertinent statutory language and legislative history leads us to conclude that Congress did not intend that the Commission impose a claim correspondence requirement on section 337 complainants." Id. at 16. In Microsphere Adhesives, as in this case, there was a correspondence between the claims infringed by the respondents and those practiced by the complainant. Nevertheless, the Commission stated that "[i]f in a future case, the products of complainant and respondents are significantly different, even though made under different claims of the same patent, we could consider the matter in the context of remedy or public interest." Id.

] FF VI 33. This corresponds with the element of claim 1 of the `752 patent reciting "one or more integrated circuit chips each having an array of Flash EEprom cells partitioned into a plurality of sectors, each sector addressable for erase such that all cells therein are erasable simultaneously." FF VI 28.

"Means for Selecting ..."

SanDisk's devices possess a "means for selecting a plurality of sectors" as specified by claim 1 of the `752 patent. As discussed above in the section on claim construction, claim 1 of the `752 patent is not limited to a device capable of selecting any combination of sectors whatsoever.

The structure of SanDisk's devices are not identical to that of the preferred embodiment disclosed in the `752 patent in connection with this means-plus-function element. However, an analysis of the SanDisk devices under the criteria set forth in Pennwalt shows that they possess an "equivalent" structure under section 112.[96]

With respect to the first aspect of the Pennwalt test relating to identical function, SanDisk's device is clearly capable of selecting "a plurality of sectors" for erase, which is all that is literally required by the patent.

[[C]

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[96] In the case of a means-plus-function claim, to determine whether a claim is met literally, one "must compare the accused structure with the disclosed structure, and must find equivalent structure as well as identity of claimed function for that structure." Pennwalt Corp. v. Durand-Wayland, Inc., 833 F.2d 931, 934 (Fed. Cir. 1987) (en banc) (emphasis in original), cert. denied, 485 U.S. 1009 (1988).

] Thus, the device performs the function of "selecting a plurality of sectors for erase."

With respect to the second aspect of the Pennwalt test, SanDisk's device possesses an equivalent structure for selecting a plurality of sectors for erase. [[C]

]

The `752 patent specification clearly contemplates the use of various types of registers, as evidenced by the specification's clear indication that Figure 3B shows only a "typical" register. See CX 1 at col. 3, lines 15-16.

Because SanDisk's devices possess an equivalent structure for selecting a plurality of sectors for erase as that described in the `752 patent, they embody this element of claim 1 of the `752 patent.

"Means for Simultaneously Performing the Erase Operation on Only the . . . Selected Sectors

[[C]

] Accordingly, SanDisk's device satisfies this claim element.

"An Individual Register Associated with Each Sector ..."

[[C]

]

Consequently, SanDisk's devices possess an individual register for holding a status to indicate whether the associated sector is selected, and thus SanDisk practices this claim element.

At a minimum, SanDisk practices the `752 patent under a doctrine of equivalents analysis. The Federal Circuit held in Hilton-Davis, 62 F.3d at 1521-22, that "a finding of infringement under the doctrine of equivalents requires proof of insubstantial differences between the claimed or accused products or processes." The Court held further that while the old "function-

way-result test" will often suffice to show the extent of differences, the trier of fact may consider other factors, including "whether persons reasonably skilled in the art would have known of the interchangeability of an ingredient not contained in the patent with one that was." Id. at 1519. Infringement under the doctrine of equivalents is an issue of fact. Id. at 1522.

[[C]

97

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97 [[C]

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Finally, SanDisk's individual register produces the same result as the register disclosed in the `752 patent. An individual register in a SanDisk device holds a status to indicate whether its associated sector is selected or not. FF VI 56. [[C]

]

OUII argues that because the sector select latch and erase latch can operate independently of each other, they do not comprise a single register per sector. However, the Staff wholly ignores the function-way-result test for infringement under the doctrine of equivalents when it argues that since "the sector select latch and the erase latch can operate independently of each other" they cannot comprise a "single register per sector."

[[C]

] See FF VI 46. When the latches are used in the SanDisk devices, they perform substantially the same function in substantially the same way to achieve substantially the same result as the registers in the `752 patent. See Graver Tank, 339 U.S. at 609. Indeed, they perform the exact function required by the claim language. Equally as important is the fact that persons skilled in the art have known of the interchangeability of SanDisk's two latch registers and the single latch register depicted in the `752 patent. See Hilton-Davis, 62 F.2d at 1519. [

[C]

]

Therefore, for the reasons stated above, it is found that SanDisk practices claim 1 of the `752 patent at least under the doctrine of equivalents.

Claim 2

As required by claim 2 of the `752 patent, the "simultaneously erasing means" in SanDisk's flash memory devices is "responsive to the status in each of the individual registers, such that only the selected sectors are included in the erasing." FF VI 57. [[C]

]

Therefore, SanDisk's devices literally satisfy this claim element, and practice claim 2 of the `752 patent.

Claim 4

[[C]

] This feature of the SanDisk devices corresponds with the requirement of claim 4 that: "all of the individual registers are simultaneously resettable to a status indicating the associated sectors as not selected." See FF VI 59.

Therefore, SanDisk literally practices claim 4 of the `752 patent.

The `338 Patent

In order to satisfy the domestic industry requirement with respect to the `338 patent, Complainant SanDisk asserts that it practices claim 27 of the `338 patent.

There is no dispute that SanDisk's flash memory devices contain the claim 27 preamble, the erase electrode element, the floating gate element, the parallel programming means, and the inhibit means.[98] See FF VI 63-66, 78-81, 89-90. Additional claim elements, which are in dispute, are discussed below.

The Increment/Decrement Element

As discussed in the claim construction section, the increment/decrement element is properly interpreted to cover a cell that achieves the programmed state by increment of the charge level with successive applications of programming voltage conditions, or a cell that achieves the erased state by decrement of the charge level with successive applications of erasing voltage conditions (or a cell that can perform both of these functions).

[[C]

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[98] In addition, SanDisk adduced evidence showing that its devices practice the inhibit means. See FF 89-90.

] Accordingly, SanDisk's devices satisfy the increment/decrement element.

The Temporary Storage Means Element

As discussed in the claim interpretation section, the function recited in claim 27 of "temporarily storing a chunk of data for programming a plurality of addressed cells", properly construed, requires that the data for each cell be stored impermanently, but at least long enough to complete the programming of that cell. [[C]

]

SanDisk's devices also use the same or equivalent structures to those disclosed in the `338 patent for performing this function. In particular, [

]

Accordingly, SanDisk's devices practice this claim element.

The Verify Means

Respondents and OUII argue that SanDisk does not practice this claim element. Their arguments are based primarily on their interpretation of this claim element to require any device covered thereunder to verify whether a cell is programmed or unprogrammed. As discussed in more detail in the claim interpretation section, the function recited in claim 27 of "verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data" is properly understood to refer to the process of determining whether the data in a cell matches the data that is targeted to be written to the cell. Since all cells in a EEprom device start in an erased state, this claim is not construed to require "verification" that a cell has not been programmed. Such a function is unnecessary in a binary device.[99]

SanDisk adduced evidence through its expert that its flash memory devices perform this function as properly construed.[100] FF VI 82.

Furthermore, SanDisk's devices use equivalent structures to those disclosed in the `338 patent for performing the verify function. In particular, [[C]

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[99] As discussed, supra, in the section on claim construction, the `338 patent reads on a binary device in accordance with the plain language of claim 27 and as supported by the specification.

[100] Mr. Thomas, Samsung's expert on the domestic industry issue, conceded in his First Supplemental Expert Report that SanDisk "verifies programming" in its flash memory devices, and confirmed in his testimony at the hearing that the SanDisk devices [[C]]

[101]

]

Therefore, SanDisk's devices practice this element of claim 27 of the `338 patent.

SanDisk Practices the Final Means-Plus-Function Element

SanDisk's flash memory devices perform the function of "further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly," using equivalent structures to those disclosed in the `338 patent. FF VI 91-94.

[[C]

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[101] [[C]

]

Conclusion on the Domestic Industry Issue

For the reasons stated above, the Administrative Law Judge determines that Complainant SanDisk satisfies the domestic industry requirement of section 337.

FINDINGS OF FACT

I. BACKGROUND

A. The Parties and the Patents

1. Complainant Corporation ("SanDisk") is a Delaware corporation with its principal place of business at 140 Caspian Court, Sunnyvale, California 94089. Stip. No. 1, Respondents' Pre-Hearing Statement at 7; Complainant's Proposed Finding of Fact 1. SanDisk recently changed its name from SunDisk Corporation to SanDisk Corporation. Harari, Tr. 6-7. SanDisk designs, develops, manufactures and sells data storage products, including flash memory circuits. Harari, Tr. 21-22. SanDisk is the assignee of the patents at issue in this investigation: U.S. Letters Patent 5,418,752 and U.S. Letters Patent 5,172,338. CX 1 (the `752 Patent); CX 2 (the `338 Patent); Stip. Nos. 2 and, Respondents' Pre-Hearing Statement at 7; Complainant's Proposed Finding of Fact 3 and 4.

2. Respondent Samsung Electronics Co., Ltd. ("SEC") is a corporation incorporated under the laws of South Korea with its principal place of business in Seoul. SEC manufactures and sells flash memory data storage products, including the accused flash memory circuits, which are imported and sold in the United States. Stip. Nos. 1-2, Respondents' Pre-Hearing Statement at 7.

3. Samsung Semiconductor, Inc. ("SSI") is a California corporation with its principal place of business in San Jose, California. SSI and SEC are related and affiliated companies. SSI is in the business of importing, marketing and selling in the United States flash memory circuits made by SEC. Stip. Nos. 1-2, Respondents' Pre-Hearing Statement at 7.

4. U.S. Patent No. 5,418,752 is entitled "Flash EEPROM System With Erase Sector Select," and issued on May 23, 1995. CX 1.

5. U.S. Patent No. 5,172,338 is entitled "Multi-State EEPROM Read And Write Circuits And Techniques," and issued on December 15, 1995. CX 2.

B. Technological Background

6. EPROM is an acronym for electrically programmable read only memory. Harari, Tr. 289.

7. An EPROM can be erased by exposure to ultraviolet light. Harari, Tr. 289.

8. EEPROM (or EEprom), or E^2PROM (so-called "E-squared prom") stands for electrically erasable programmable read only memory. Harari, Tr. 9, 40, 289.

9. With an EEPROM an electrical erase function is used. Harari, Tr. 289

10. Like hard disk mechanical memory, both EPROM and EEPROM semiconductor memories are said to be "nonvolatile" because they retain information even when their power is off. In contrast, volatile RAM ("random access memory") technologies like SRAM ("static RAM"), and the less expensive DRAM ("dynamic RAM"), require a continuous supply of power in order to preserve information. Tutorial (Harari) Tr. 15-17.

11. With respect to the SRAM, once the information is written on the memory, it remains there as long as the power remains. In the DRAM, the memory has to be refreshed every few milliseconds. Tutorial (Harari) Tr. 15-16.

12. The term "flash" in "flash EEPROM refers" to the quick speed of the erasing operation. Harari, Tr. 37.

13. In a flash EEPROM, the flash memory cells are transistors. Tutorial

(Harari) Tr. 47; Tutorial (Frey) Tr. 94-95.

14. In each transistor there is a source, a gate and a drain. Tutorial (Frey) Tr. 95-96.

15. In an EPROM or EEPROM cell, there is a floating gate which consists of a metal or conducting region that lies between the substrate of the cell and what is called the control gate. The floating gate is surrounded by a sea of oxide insulator. The transistors are a type of metal oxide semiconductor field effect transistors, or MOSFETs. Tutorial (Harari) Tr. 50; Tutorial (Frey) Tr. 95-97; RPX 204.

16. The source and the drain are electron-enriched regions located to either side of the gate. Tutorial (Harari) Tr. 50; Tutorial (Frey) Tr. 95, 98-99, 101.

17. There are two ways of getting electrons from the substrate to the floating gate. One method is hot electron injection (or "HEI"), and the other is Fowler-Nordheim tunneling or programming. Tutorial (Harari) Tr. 51-52; Tutorial (Frey) Tr. 105.

18. The HEI method uses the control gate above the floating gate and substrate. The control gate provides a means of accessing the transistor for reading and programming. There is no contact between the floating gate and the control gate except through capacitance. To program a transistor a high electric field or voltage such as 7 volts is applied to the drain, zero volts is applied to the source and 12 volts is applied to the control gate. The electrons are thus accelerated to the point at which some of them cross the glass to be captured on the floating gate. The electrons will generally remain there until they are removed. Tutorial (Harari) Tr. 51; Tutorial (Frey) 108-109; RPX 208.

19. To erase a cell that has been programmed using the HEI method, one

uses Fowler-Nordheim tunneling, which is based on a quantum mechanical phenomenon. One must set up the proper electric field for erasing, or one may reverse the electric field and cause the electrons to move in the opposite direction for programming. Tutorial (Harari) Tr. 53.

20. In Fowler-Nordheim programming, a very high voltage to the gate of the device brings electrons close to the surface and increases the probability of being able to measure electrons in the floating gate. The technique relies on the tunneling of electrons thorough material that which is normally thought of as an insulator. When the high voltage is taken off, electrons are stuck on the floating gate. The presence of the electrons on the floating gate affects the flow of current from source to drain. Tutorial (Frey) Tr. 107-108; RPX 207.

21. To erase using a Fowler-Nordheim technique with devices that were built for Fowler-Nordheim programming, and thus do not have thick oxide layers, one simply reverses the voltages to effect erasure. Electrons tunnel from the substrate to the gate or from the gate to the substrate depending on whether one wishes to program or erase. Some companies (other than SanDisk and Samsung) perform Fowler-Nordheim tunneling though the source or the drain, in which case they do not use simple EEPROM cells. Tutorial (Frey) Tr. 111-112; RPX 210.

22. To erase using the Fowler-Nordheim technique with devices that were not built for Fowler-Nordheim programming, and which have thick oxide and for which one has used HEI, one uses an electrode for erasing. The electrode may be placed in various regions, for example, on the side of the floating gate, or overlapping the floating gate. The electrode acts to remove the electrons from the floating gate. Tutorial (Frey) Tr. 112-113.

23. If the transistor is "on," current will be conducted across the transistor through the channel from the source to the drain. If the transistor is "off," current will not be conducted across the transistor. Tutorial (Harari) Tr. 48.

24. Therefore, a memory cell in an EEPROM may operate in a binary system in which, depending on whether there is a charge on the floating gate or not, the current flows through the cell or not. Tutorial (Frey) Tr. 103. Each transistor, or flash memory cell, can be on or off, and can thus store a 0 (zero) or a 1. Tutorial (Harari) Tr. 47. Either state may be called 0 or 1, as long as the use of the terms is consistent. Tutorial (Frey) Tr. 103.

25. In the "unprogrammed" state, current flows as electrons are attracted across the channel to the drain. A cell is said to be "programmed" when there is a negative charge on the floating gate, which repels electrons, and makes it harder for current to flow from the source to the drain. Tutorial (Frey) Tr. 100-102.

26. There are various methods of reading a cell to determine whether it is programmed (with no current flowing through it) or unprogrammed. Tutorial (Frey) Tr. 101-102.

27. One could read a cell with a sense amplifier in which the current is compared with the current that one would expect to flow in a cell that is not programmed. The actual current that would flow through a cell is very small. If the sense amplifier senses current, it compares that current, and then creates a large output signal. Thus it is called a "sense amplifier." Tutorial (Frey) Tr. 102.

28. Another method of reading a cell is simply to determine whether current flows or not, in contrast to comparing the current against

another signal. Tutorial (Frey) Tr. 101-102.

29. EEPROM cells can also be used for multistate storage, or multilevel storage, in which rather than reading a cell as merely on or off -- unprogrammed or programmed -- a cell has additional individual states. Therefore, rather than each cell having a zero and a one, which constitutes one bit of information, a cell can have two, three, four or more bits. Tutorial (Harari) Tr. 75-77.

30. Multistate storage requires very precise and accurate programming to the various individual states. Tutorial (Harari) Tr. 76. Multistate devices are not currently in commercial use. Tutorial (Frey) Tr. 124.

31. The term "architectural definition" refers to the concept of a memory, and matters such as how it works: how one addresses it; how many bits constitute its inputs and outputs; how one obtains data from it; how addressing is done within the memory; and if there is a problem, how the problem is solved. Thomas, Tr. 1468.

32. There are a number of different types of cell architectures that can be used to produce flash memories, among them are NOR (which is used by SanDisk), and NAND (which is used by Samsung). Harari, Tr. 120-121.

33. The term "array" can be used to refer to a set of rows and columns of addressable EEPROM cells. Harari, Tr. 65.

34. Two typical connections for cells in an EEPROM or flash EEPROM are NOR and NAND. Tutorial (Frey) Tr. 114.

35. With the NOR connection, there are three connections to each cell. One can thus have independent control of the source, the drain or the gate with any of the cells. Tutorial (Frey) Tr. 114.

36. NOR derives from standard logic terminology, and stands for "not or," an inverted OR signal. Tutorial (Frey) Tr. 115.

37. If, for example, three cells A, B and C are connected in a row as NOR cells, and there is one line to put current in, and other line to determine whether there is current out, a sense amplifier or other device will indicate that there is current out if just one of the cells A, B or C acts as closed switch. Tutorial (Frey) Tr. 115; RPX 211; RPX 212.

38. With the NAND (derived from the standard logic terminology "not and") connection, the cells are connected in series. One can make the source of one cell equal to the drain of the another cell. Current will flow to the output only if all the cells (for example, A, B, C and so) on are closed. Tutorial (Frey) Tr. 115-116; Tutorial (Harari) Tr. 49; RPX 213; RPX 214.

39. NAND cells take up less space on a chip than NOR cells. Tutorial (Frey) Tr. 116-117.

40. With NAND connections, one does not have to access the individual nodes as with NOR connections. Tutorial (Harari) Tr. 49. However, one does not have individual control of each NAND cell. Tutorial (Frey) Tr. 116-117. Thus, one may program NOR and NAND cells differently. Tutorial (Frey) Tr. 116-119.

41. "VLSI" is the acronym for very large-scale integrated circuits. The term came into being after chips started having more than 10,000 gates. McGreivy, Tr. 1648-1649. Currently, commercial flash EEPROMs have millions of cells, e.g. 16 or 32 million. Tutorial (Harari) Tr. 46-47; Tutorial (Frey) Tr. 94-95.

42. Flash memory circuits are typically attached to a circuit board with other circuitry and are often contained within a sealed enclosure which is then attached to or installed within a particular application. SPFF

33; Complainant's Resp. to Proposed Findings of Fact at 172.

43. A controller is used to address an array of flash memory chips. Harari, Tr. 137. A controller can be used with flash chips to mimic (or emulate) a disk drive. Harari, Tr. 46, 137. In that case, there is a significant amount of file management of the cells on the chips. Harari, Tr. 137.

44. Instead of using a hardware controller, some companies use software that tells the host microprocessor how to address the flash memory chips. Harari, Tr. 137, 141.

45. In addition to using less power than other memory products such as disk drives, flash memory circuits have no mechanical moving parts and are consequently more rugged. Harari, Tr. 84-86.

46. Endurance, or fatigue, is a consideration associated with EPROM and EEPROM semiconductor technology because programming and erasing operations cause electrons to become trapped in, and permanently damage, the silicon dioxide (i.e., glass) layer surrounding the floating gate. Tutorial (Harari) Tr. 62-71; Harari, Tr. 24-25; CPX 28. The resulting fatigue causes the voltage "window" between the erased and programmed states to close before the device ultimately fails. Tutorial (Harari) Tr. 69-70; Harari, Tr. 24-25; CPX 29; CX 2, Fig. 8 (discussed at col. 9, line 53 - col. 10, line 15).

47. Fatigue was addressed at the chip level through individually erasing only selected sectors of the array and through inhibiting further programming of correctly verified cells. Harari, Tr. 38; CPX 32 described at Tutorial (Harari) Tr. 77-79. Other approaches to maximizing the endurance of flash EEPROM at the controller, or system, level included wear-out leveling, dynamic mapping of defective cells,

and error correcting codes. Tutorial (Harari) Tr. 79-81; CPX 32.

48. Since solid state devices are traditionally much faster than mechanical devices, it was important for any so called "flash-disk" system for replacing hard disk drives in mobile computers to be at least as fast as conventional mechanical mass storage devices. Harari, Tr. 30-31. The slower write and erase performance characteristics of conventional flash EEPROM devices were addressed through the programming of cells in parallel and the simultaneous erasing of multiple sectors of cells. CX 2, Fig. 6 described at col. 8, line 63 - col. 9, line 23, and Fig. 14 described at col. 19, lines 27-41; Harari Tr. 38, lines 13-15.

49. SanDisk offered its first commercial, flash-based mass storage product in 1991. Harari, Tr. 87. Eventually, SanDisk, Toshiba, Samsung, and to a lesser extent Intel, have become the largest suppliers of mass data storage flash memory products. Tutorial (Harari) Tr. 41; CPX 13 and 14.

50. AMD, SGS, and Intel have concentrated mainly on code storage flash memory products, like the "Basic Input Output System," or BIOS, chip used to store start-up information in many personal computers. Tutorial (Harari) Tr. 40-41; CPX 13 and 14; Harari Tr. 133-134.

51. "Technology transfer," as used in this investigation, is the concept of taking a system that has been made in a research and development laboratory and transferring it for commercial production to a fabrication facility. One has to combine the design with the process that is available at the fabrication facility so that the design works as it is supposed to work. The fabrication facility will have process limitations and the design will have its own limitations. Therefore, technology transfer is the interrelation of the technology and/or the design and the technology. Thomas, Tr. 1468-1469.

52. Generally, changing the process is more difficult than changing the design, because the process is used for a number of different products. This makes it difficult to get the process engineers at the fabrication facilities to change their process(es). Therefore, generally, the designs are modified to assure that they will work with the process. Thomas, Tr. 1469.

53. "Qualification" is a process by which a customer and the manufacturer make sure that the products meet all of the specifications under the working conditions for the product. Qualification requires a detailed understanding of how a product operates and how it works in the customer's system. Failures must be completely analyzed, and corrective action must be taken by the manufacturer. Thomas, Tr. 1465-1466.

II. IMPORTATION AND SALE

1. Respondents have imported or are importing at least the following products into the United States: [

[C]

] CX 165C at 2-16, 24-38; CX30C to CX-34C; CX-41C.

2. Respondents are selling or have sold at least the following products after such products have been imported into the United States: [

[C]]

CX 165C at 45-60; CX 35C to CX 40C.

3. [

[C]

] Choi, Tr. 1205-1205, 1394; CX 193C (Ali Dep.) at 388, 395.

4. [

[C]

] CX 155C (Samsung interrogatory responses) at 2-3.

5. [

[C]

] Choi, Tr. 1391.

6. Respondents have not provided any documentary evidence that they are importing [

[C]

] Choi, Tr. 1390-1399; CX 155C at 2-3; see generally CX 30C to

CX 41C.

III. CLAIM CONSTRUCTION

A. Construction of Claims 1, 2 and 4 of the `752 Patent

1. Claim 1 of the `752 patent is as follows:

> A Flash EEprom system comprising:
>
> one or more integrated circuit chips each having an array of Flash EEprom cells partitioned into a plurality of sectors, each sector addressable for erase such that all cells therein are erasable simultaneously;
>
> means for selecting a plurality of sectors among the one or more chips for erase operation;
>
> means for simultaneously performing the erase operation on only the plurality of selected sectors; and
>
> individual register associated with each sector for holding a status to indicate whether the sector is selected or not.

CX 1/RX 2 (`752 Patent) at col. 16, line 59 - col. 17, line 3.

2. Neither the word "controller" nor any similar word is found in the preamble or in any other portion of claim 1. CX 1.

3. The first reference to a "controller" in the patent specification occurs in the "Summary of the Invention," as follows:

> According to one aspect of the present invention, an array of Flash EEprom cells on a chip is organized into sectors such that all cells within each sector are erasable at once. A Flash EEprom memory system comprises one or more Flash EEprom chips under the control of a controller.

CX 1 at col. 1, lines 62-67 (emphasis added).

4. According to the specification, a "computer system in which various aspects of the present invention are incorporated is illustrated generally in FIG. 1A." CX 1 at col. 3, lines 34-36.

5. The specification further explains that "[t]he bulk storage memory 29

is constructed of a memory controller 31, connected to the computer system bus 23, and an array 33 of EEprom integrated circuit chips." CX 1 at col. 3, lines 61-64.

6. The specification also states that in "FIG. 1B, the controller 31 is preferably formed primarily on a single integrated circuit chip. It is connected to the system address and data bus 39, part of the system bus 33, as well as being connected to the system control lines 41, which include interrupt, read, write and other usual computer system control lines." CX 1 at col. 4, lines 3-8. See also CX 1 at col. 4, lines 27-36 (stating that for large amounts of memory, additional EEprom arrays can be connected to the serial data lines of the controller chip.)

7. In connection with Fig. 2, which like Figs. 1A and 1B also depicts a controller, the specification states that "A Flash EEprom system includes one or more Flash EEprom chips such as 201, 203, 205. They are in communication with a controller 31 through lines 209. Typically, the controller 31 is itself in communication with a microprocessor system (not shown)." CX 1 at col. 5, lines 6-12.

8. The specification states at col. 5, lines 26-42, as follows:

> FIG. 3A illustrates a block diagram circuit 220 on a Flash EEprom chip (such as the chip 210 of FIG. 2) with which one or more sectors such as 211, 213 are selected (or deselected) for erase. Essentially, each sector such as 211, 213 is selected or tagged by setting the state of an erase enable register such as 221, 223 associated with the respective sectors. The selection and subsequent erase operations are performed under the control of a controller 31 (see FIG. 2). The circuit 220 is in communication with the controller 31 through lines 209. Command information from the controller is captured in the circuit 220 by a command register 225 through a serial interface 227. It is then decoded by a command decoder 229 which outputs various control signals. Similarly, address information is captured by an address register 231 and is decoded by an address decoder 233.

9. The Figures and the corresponding "Defect Mapping" portion of the specification were intended to support several claims that appeared in the patent application as originally filed, but which were subsequently canceled by the applicants as directed to a non-elected invention. See CX 6 at SD008688-8693, SD008733, SD008736.

10. "A" refers or to an "undetermined, unidentified, or unspecified" noun. Webster's Third International Dictionary 1 (1976) ("Webster's").

11. A "plurality" in its most common meaning is "the state of being plural," i.e., "relating to or consisting of or containing more than one ...." Webster's at 1745.

12. Early in the specification, the following is stated:

> The invention allows any combination of sectors to be selected and then erased simultaneously. This is faster and more efficient than prior art schemes where all the sectors must be erased ever[y]time or only one sector at a time can be erased. The invention further allows any combination of sectors selected for erase to be deselected and prevented from further erasing during the erase operation.

CX 1 at col. 1, line 67 through col. 2, line 6.

13. As originally filed, Application No. 07/963,851, which led to the '752 patent, contained 62 claims. CX 6 at SD008655-008703.

14. Most of the original claims (original claims 2, 3 and 10-62) were canceled at the outset of the prosecution as part of the Divisional Application Transmittal. CX 6 at SD008712.

15. Of the original claims that remained (original claims 1, and 4-9), original claims 6 through 9 formed the basis of all final claims (i.e., claims 1-4) of the '752 patent as issued. CX 6 at SD008726, SD008737, SD008751.

16. Eventually, all other claims remaining in the application were canceled at the applicants' request. CX 6 at SD008775.

17. In the Examiner's first Office Action, which was dated January 25, 1993, he rejected original claims 1, 4 and 5, and objected to original claims 6 through 9. The Examiner objected to claims 6 through 9 only because they were dependent upon original claim 1, which he rejected under 35 U.S.C. § 102(a). However, he stated that if claims 6 though 9 were written in independent form, and included all of the limitations of the base claim (i.e., original claim 1) and any intervening claims, then original claims 6 through 9 would be allowable. CX 6 at SD008727.

18. In an Amendment dated May 24, 1993 and received by the PTO on May 27, 1993, the applicants, through their patent agent, added new claims 63 through 66, which were based on original claims 6 through 9 yet written so as not to depend from original claim 1. CX 6 at SD008733, SD008737-008738.

19. In the Remarks made in connection with the May 27, 1993 Amendment and in other filings at the PTO, the applicants continued to seek allowance of original claims 1, 4 through 5, as well as original claims 6 through 9 (in their original, dependent form) until, in an Amendment dated September 14, 1994 and received by the PTO on September 19, 1994, they canceled original claims 1, and 4 through 9. CX 6 at SD008761, SD008774-008776.

20. The prosecution history shows that added claims 63 through 66 issued as the claims of the `752 patent without any amendment and without any substantive remarks concerning those added claims. See SD008764, SD008775-008776, SD008777 (Notice of Allowability, dated Nov. 21, 1994).

21. In an Amendment received by the PTO on May 27, 1993, applicants added claims 63 through 66, and, among other things, amended original claim 1 in an effort to obtain its allowance. Original claim 1 was amended to add the following limitation: "a bus for accessing said plurality of sectors." CX 6 at SD008733. Original claims 1, 4 and 5 had been rejected by the Examiner as anticipated by Sparks et. al. SD008727. Thus, in connection with the May 27, 1993 Amendment it was stated that "[c]laim 1 is being amended to more clearly distinguish over Sparks et al." CX 6 at SD008737. The Remarks continued by stating that claim 1 "recites a Flash EEPROM system having a plurality of erasable sectors addressable by a bus, and means for selecting and simultaneously erasing an arbitrary selection of sectors thereamong, the plurality of erasable sectors may be from one IC chip or pooled from several chips." CX 6 at SD008737 (emphasis added).

22. The word "arbitrary" ordinarily conveys the concept of randomness or choice. See Webster's at 110.

23. It is not clear whether this new limitation played any role in the patent agent's decision to characterize the selection of sectors as "arbitrary" in the same sentence in which he also stated that the claimed Flash EEPROM system had "a plurality of sectors addressable by a bus." See CX 6 at SD008737.

24. The Examiner found that the amendment adding the new limitation of a "bus" had made the question of how the claimed invention operated "confusing," and asked: "Does the selecting means utilize the bus to select the plurality of sectors? Does the performing means use the bus or the selecting means to perform the erase operation?" CX 6 at SD008752.

25. Finally, the patent agent, on behalf of applicants, removed the amendment from original claim 1, and eventually canceled the claim. CX 6 at SD008761, SD008776.

26. Another Amendment dated February 24, 1994 was received by the PTO on February 25, 1994. In that Amendment, the applicants through their patent agent removed the new claim limitation discussed above concerning a bus, which was added in the May 27, 1993 Amendment. The patent agent also, inter alia, set forth additional arguments to differentiate the claimed invention of original claim 1 from the prior art, particularly the Sparks et al. reference. The patent agent pointed out that Sparks et al. disclosed splitting the EEPROM array into two or more subarrays such that each subarray is configured and accessed as a separate memory chip. CX 6 at SD008760-008763.

27. In connection with the February 25, 1994 Amendment, Sparks et al. was differentiated from the claimed invention of original claim 1 as follows:

> Each time either a single chip can be selected for erase or all the chip can be selected for bulk erase. There is no provision as in Applicants' amended claim 1 for further partitioning each chip into flash sectors and allowing any combination of flash sectors within a chip or among all the chips of a memory system to be erased together. That is, Sparks et al. do not anticipate each chips "partitioned into a plurality of sectors, each sector addressable for erase such that all cells therein are erasable simultaneously; means for selecting a plurality of sectors among the one or more chips for erase operation; and means for simultaneously performing the erase operation on only the plurality of selected sectors.

CX 6 at SD008762.

28. On June 9, 1994, the patent agent had a personal interview with the Examiner. According to the Examiner's general description of the

interview, "[t]he prior art was discussed and Mr. Yau [the patent agent] pointed out that none of the references disclosed a means for selecting a plurality of sectors among the IC chips." CX 6 at SD008771.

29. Claim 1 of the `752 patent contains a limitation found initially in original claim 6, i.e., the fourth and last element recited in claim 1, an "individual register associated with each sector for holding a status to indicate whether the sector is selected or not." At the time that the Examiner indicated the allowability of original claim 6, that limitation was the only difference between dependent, original claim 6 and independent, claim 1 as originally filed. CX 6 at SD008687-008688, SD008761.

30. The third recited element in the body of claim 1 is a "means for simultaneously performing the erase operation on only the plurality of selected sectors." CX 1.

31. The structures which correspond to the erase means described claimed in the third element of claim 1 are the registers and the associated erase enable command. The erase of a sector is conditional upon the status that is stored in its associated individual register. See Guterman, Tr. 563-564; Harari, Tr. 232.

32. The structures corresponding to the third recited element of claim 1 of the 752 patent are found in Figs. 3A and 4 (item 5), and the portions of the specification that describe those Figures. See, e.g., CX 1 at col. 6, lines 3-29; Mehrotra, Tr. 379-380.

33. The fourth, and final element recited in the body of independent claim 1 of the `752 patent is an "individual register associated with each sector for holding a status to indicate whether the sector is selected or not." CX 1.

34. The most common meaning for the adjective "individual" is "of, belonging to, arising from, or possessed by, or used by an individual." Synonyms for the adjective "individual" are "characteristic" and "special." Webster's at 1152.

35. The term "register" is well understood in the semiconductor industry to mean circuitry that stores information, typically on a temporary basis. Harari, Tr. 61; Guterman, Tr. 448. It is common for a register to be implemented by setting more than one latch to store the information. Harari, Tr. 61-63; Mehrotra, Tr. 316; Guterman, Tr. 448, 552-553; CX 198.

36. Claim 2 of the `752 patent is as follows:

> The Flash EEprom system according to claim 1, wherein the simultaneously erasing means is responsive to the status in each of the individual registers, such that only the selected registers are included in the erasing.

CX 1/RX 2 (`752 Patent), at col. 17, lines 4-7.

37. Claim 4 of the `752 patent is as follows:

> The Flash EEprom system according to claim 1, wherein all the individual registers are simultaneously resettable to a status indicating the associated sectors as not selected.

CX 1/RX 2 (`752 Patent), at col. 18, lines 4-7.

38. The `752 patent discloses the preferred embodiment of the invention of claim 4 in Figure 3A. In the preferred embodiment, a reset signal is provided simultaneously and globally to all of the erase enable registers, resetting each register to "0," which is the nonselected status. See Allen, Tr. 1102; Complainant's Reply FF 87-88.

B. **Construction of Claim 27 of the `338 Patent**

39. Claim 27 of the `338 patent is as follows:

> In an array of addressable semiconductor electrically erasable and programmable memory (EEprom) cells on an integrated circuit chip, the memory cell being of the type having a source, a drain, a control gate and an erase electrode receptive to specific voltage conditions for reading, programming and erasing of data in the cell, and having a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell, such that a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions, a system for programming data to EEprom cells including means for temporarily storing a chunk of data for programming a plurality of addressed cells, means for programming in parallel the stored chunk of data into the plurality of addressed cells, and means for verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data, wherein the improvement comprises:
>
> means for inhibiting further programming of correctly verified cells among the plurality of addressed cells; and means for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly.

CX 2/RX 5 (`338 Patent) at col. 26, lines. 28-54.

40. The term erase electrode" is found in the `338 patent only in the claims. CX 2; see CFF 257; SFF 98.

41. The term "electrode" is commonly understood in the semiconductor industry as a terminal to which an electrical signal is applied to perform some function. Pathak, Tr. 792, 918.

42. An "erase electrode" is understood in the semiconductor industry as a terminal to which erase voltage conditions are applied to draw electrons off the floating gate. Pathak, Tr. 792.

43. Various structures or terminals in a flash memory device can function

also as an erase electrode as that term would be commonly understood, including the silicon substrate. Harari, Tr. 77-83.

44. Various companies have used the substrate instead of an erase gate as the terminal to which erase voltage conditions are applied to draw electrons off the floating gate during the erase operation. Harari, Tr. 77-83; CPX 25.

45. The word "or" in this instance serves its normal function of indicating the availability of an alternative or a choice. See Webster's at 1585.

46. The increment/decrement element of the preamble of claim 27 corresponds to the programming algorithm illustrated in Fig. 15 (item 6), which is described in the text at col. 19, line 57 through col. 20, line 16), whereas the erasing algorithm is illustrated separately in Fig. 11 (items 1 and 2), which is described at col. 16, lines 18-25.

47. The preferred embodiment disclosed in the specification provides examples of incremental programming and of incremental or decremental erasing. See CX 2 at col. 18, lines 21-29.

48. The application of voltage conditions for programing and the application of voltage conditions for erasing are independent of each other. Harari, Tr. 1861, 1870.

49. In both binary and multistate devices, one may design for incremental programming and/or for incremental erasing. However, programming and erasing are not part of the same operation. Harari, Tr. 1869; Pathak, Tr. 937.

50. The consequences of over-erasing are endurance-related. The effect of over-erasing, even in a multistate device, is not catastrophic to the performance of the device. Harari, Tr. 1870; Guterman, Tr. 577-578.

51. With respect to the '338 patent, after the programming of a cell is completed, the information used to program that cell is not used again. Harari, Tr. 248-249.

52. The term "temporarily" ordinarily means "for a brief period: during a limited time: briefly." Webster's at 2353.

53. The "temporarily storing" means of claim 27 is disclosed in Figure 5, including block 190 (labeled "Read/Program Latches and Shift Registers"). Harari, Tr. 247-249; Thomas, Tr. 1509-1511; CX 2, at col. 19, line 27 through col. 20, line 36.

54. The data may be stored in the latches until verification has occurred for the entire chunk of data stored therein, although there is no express requirement to that effect. Thomas, Tr. 1510-1511; Pathak, Tr. 939.

55. After a particular cell to be programmed is verified, the data stored in the latch 190 serves no function for the cell that is already programmed, while the programming continues for the rest of the chunk. Harari, Tr. 247-249; Mehrotra, Tr. 329; Guterman, Tr. 587-588.

56. One of ordinary skill in the art knows that once programming and verification has taken place, the job is done, and "temporarily" in that case would mean just until the job is done. Pathak, Tr. 940-944.

57. Figure 14 of the '338 patent discloses certain structures with which the parallel programming function required by the preamble of claim 27 can be performed. CX 2 at col. 5, lines 40-41; col. 19, lines 27-41; Mehrotra, Tr. 330.

58. In particular, Figure 14 shows an embodiment in which a Program Circuit with Inhibit, block 210, performs the parallel programming function, with the source multiplexer (or "mux") 107 and the drain mux

109 providing the data path. CX 2 at col. 19, lines 27-41; Mehrotra, Tr. 330-334.

59. The cells in the preferred embodiment of the `338 patent are connected in a NOR architecture configuration. Pathak, Tr. 812-813.

60. HEI programming is thus appropriate for use with the cells described in the preferred embodiment. Harari (Tutorial), Tr. 51-52; Mehrotra, Tr. 334-335.

61. The language of claim 27 is silent on the cell structure and the corresponding programming method that must be used. It merely recites the broad, general function of "programming in parallel" without specifying how that programming occurs. One of ordinary skill in the art would know that parallel programming can be achieved through more than one method depending on the type of cell structure selected in a device. Furthermore, circuit designers are familiar with the various methods of programming cells depending upon their structures. Pathak, Tr. 944-946; Harari, Tr. 1861-1865.

62. In claim 27 of the `338 patent, "programming in parallel" means that programming takes place for more than one cell at a time, such that all cells selected for programming by a chunk of data receive programming conditions at the same time. See Harari, Tr. 76; Pathak, Tr. 807-808; CX 2 at col 19, lines 30-31 ("The EEprom array 60 is addressed by N cells at a time.").

63. The term "verifying" as it is used in claim 27 of the '338 patent normally would be understood by one of ordinary skill to refer to the process of determining whether the data in a memory cell matches the data that is targeted to be written into the cell. Guterman, Tr. 489-490, 499. There is no contrary definition of the term in the `338

patent. CX 2.

64. Mr. Thomas, Respondents' expert on whether Complainant SanDisk practices the '338 patent and on whether Samsung infringes the '338 patent, testified that the term "verify" is ordinarily used very loosely in the semiconductor industry to refer to the process of determining whether a cell is finished programming. Thomas, Tr. 1594-1595.

65. In a multi-state device, such as that described in the `338 patent's specification, a cell can be in one of several states. In performing the verification function, the first step is to determine the state of the cell to be verified (e.g., 0, 1, 2, 3). After determining the state the cell is in, the next step is to determine whether the cell is in the target state for that cell. If the cell is in the target state, the cell is verified; if not, further programming is required. Guterman, Tr. 490-493; CPX 46.

66. In a binary device, before programming can begin all cells must be in the erased state. Guterman, Tr, 493-495; CPX 48.

67. Inasmuch as all cells start in the erased state, if the targeted state of a particular cell is the erased state, then the cell is in the targeted state before the programming cycle begins, and therefore no further action needs to be taken with respect to that cell. Harari, Tr. 264-265; Guterman, Tr. 493-495, 499-503; CPX 48.

68. If the targeted state of a particular cell is the programmed state, and if the cell is not in the targeted state before the programming cycle begins, then programming pulses must be applied to bring the cell to its targeted state. Guterman, Tr. 493-495; CPX 48. For cells targeted to be in the programmed state, the cell is read after each programming pulse to verify whether the cell is in the programmed state

(i.e., reads a "1"). Once the cell is sensed to be in the programmed state, further programming to that cell is terminated. Guterman, Tr. 493-495; CPX 48.

69. Figure 11-E of the '344 patent (which is incorporated by reference into the '338 patent) discloses circuitry that corresponds to the verify means in a multi-state implementation of the claim 27 invention. Figure 11-E depicts a multi-state implementation for a single cell in which the cell is able to hold one of four states. CX 2 at col. 4, lines 23-30; Guterman, Tr. 498-499; CX 3 (the '344 Patent); CPX 64.

70. Figure 11-E of the `344 patent discloses four sense amplifiers, one associated with each of the four states that the cell can hold. Each of the four sense amplifiers senses whether the current passing through the cell is greater or lesser than the reference current corresponding to the state associated with that sense amplifier. In the multi-state embodiment disclosed in Figure 11-E, once the sense amplifiers perform their sensing operation, the results are fed into the comparator disclosed in Figure 11-E, which determines whether the state of the cell matches the targeted state of the cell. Guterman, Tr. 499-503; CX 3, Fig. 11-E.

71. A binary embodiment equivalent to that disclosed in Figure 11-E of the '344 patent would not need all the circuitry disclosed in that Figure for a multi-state implementation. Guterman, Tr. 499-503. In a binary device, it is unnecessary to have more than one sense amplifier to perform the verification function of claim 27, since the only decision or verification that the device has to make is whether the cell is in the programmed state. Guterman, Tr. 499-503; Allen, Tr. 1173; CPX 64, 66.

72. For a binary device, it would be logical for a circuit designer to simplify the structure of Figure 11-E of the `344 patent by eliminating three of the four sense amplifiers and the buffers and circuitry uniquely associated with those sense amplifiers, since they serve no function in a binary device and unnecessarily occupy surface area on the chip. Furthermore, with a single sense amplifier, it is unnecessary to have a separate comparator circuit, since that comparator would merely replicate the function of the sense amplifier. Guterman, Tr. 499-503; CPX 64; CPX 66.

73. Figure 16 of the '338 Patent discloses certain additional structures for performing the verification function in a multi-state device. In the circuit compare module 703 shown in the Figure, the read bits are compared bit by bit with corresponding program data bits, i.e., it is determined whether there is a match between the read and write data. This is performed by XOR (exclusive OR) gates such as 711, 713 and 715 shown in Fig. 16. The specification states that the number of such XOR gates used depends upon the number of binary bits encoded for each cell. The output of the XOR gates passes through a NOR gate 717 whenever all the bits are verified, and node 726 is taken high so that latch 721 is set in the verified state. Once latch 721 is set, the cell inhibited from further programming during subsequent programming pulses that may be applied on the chunk. If, however, the read data does not match the write data, then latch 721 remains in its previous state. Mehrotra, Tr. 339; CX 2 at col. 20, lines 17-51.

74. The '344 patent expressly discloses that a single sense amplifier and a single reference level can be used to differentiate between conduction states "1" (which could indicate "programmed") and "0" (for "erased").

CX 3 at col. 26, lines 55-60. The `344 patent teaches that in a four-state storage device the comparison may be accomplished with four consecutive read cycles and only one sense amplifier, with a different reference applied at each cycle, if the additional time required for reading is not a concern. CX 3 at col. 25, line 64 through col. 26, line 17.

75. The Figure 16 multi-state embodiment could be modified for a binary device by making some simplifications to the structures that would be obvious to an ordinary flash memory circuit designer. Mehrotra, Tr. 342; Pathak, Tr. 819-820.

76. The `338 patent contemplates an embodiment with only two states. The '338 Patent expressly states in the context of discussing the verification function that "if each memory cell is to store K states, then at least K - 1, or preferably K reference levels need be provided. In one embodiment, the addressed cell is compared to the K reference cells using k sense amplifiers in parallel. This is preferable for the 2-state case because of speed ...." CX 2 at col. 11, lines 56-61.

77. It would be obvious to a circuit designer of ordinary skill to eliminate all but one of the XOR gates (711, 713, 715) in a binary device, since only one bit is being stored in the cell (i.e., "L" = 1). Mehrotra, 342-343; CPX 120; Pathak, Tr. 820-822; CPX 122.

78. In a binary device, it would be obvious to a circuit designer of ordinary skill to change NOR gate 717 of the `338 patent to a single inverter, since there would only be a single XOR gate, and therefore only a single input. Mehrotra, Tr. 342-345; CPX 120; Pathak, Tr. 820-822; CPX 122.

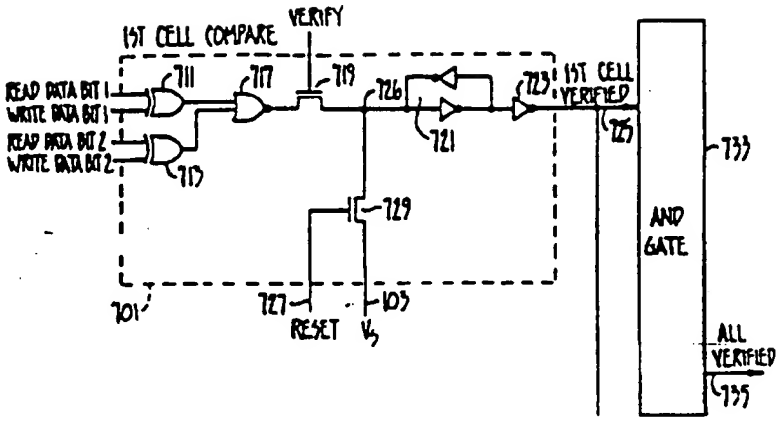
79. In implementing Figure 16 of the `338 patent in a binary device, the

possible combinations of read (R) and write (W) are greatly reduced, as compared to a multi-state device, such that it is not necessary to implement the logic inherent XOR (exclusive OR) gates and NOR gates to verify a cell. Thus, one would expect to make additional simplifications to the circuitry shown in Figure 16 by eliminating entirely the XOR gates and the NOR gate 717. Mehrotra, Tr. 345-351; CPX 120; Pathak, Tr. 819-829; CPX 122; CPX 127; CPX 128.

80. In a binary device, there are only four logically possible states: R=0 and W=0; R=0 and W=1; R=1 and W=0; R=1 and W=1. For example, in the first scenario (R=0 and W=0), the data read from the memory is zero (erased) and the data desired to be written into the memory is also zero. Note also that the third scenario (R=1 and W=0) should not be possible because all cells are required to be in an erased state before programming starts. Mehrotra, Tr. 345-346.

81. Figure 16 of the '338 patent discloses one embodiment of the compare circuit used in the multi-state, preferred embodiment. Figure 16 also discloses circuitry that inhibits further programming of the memory cells. CX 2 at col. 20, line 17-18; Mehrotra, Tr. 340.

82. The pertinent circuitry is depicted in Figure 16 of the '338 as follows:



This illustration, like the illustration contained in Respondents' reply brief, depicts the circuitry of one compare module contained in the preferred embodiment (compare module 701). Figure 16 and the text of the specification provide for "N compare modules such as 701, 703, one for each of the N cells in the chunk." CX 2 at col. 20, lines 18-20, Fig. 16.

83. In the circuit shown in Figure 16, a latch 721 performs the function of inhibiting further programming to correctly verified cells. Mehrotra, Tr. 340-342.

84. When a cell is correctly verified, the result is sent to latch 721, which is then set to the verified state. Mehrotra, Tr. 340; CX 2 at col. 20, lines 28-32.

85. The specification mentions that at the end of a programming pulse all the latches are reset to the unverified state. Node 726 can only be reset by transistor 729 and not by node 717 after node 726 goes high. Mehrotra, Tr. 371-372. Once latch 721 is set in the verified state, the cell is inhibited from further programming during any subsequent

programming pulses which may be applied. Latch 721 in Figure 16 is a "one-way latch." Mehrotra, Tr. 340.

86. The `338 patent specification teaches that "[p]rogramming and verification are repeated until all the cells are correctly verified." FIG. 15(7). Thus, each cell must be read to determine whether the read and write data for that cell match. The specification does not teach that the verification process is to occur repeatedly, i.e., after a cell has been verified. CX 2 at col. 20, lines 14-16.

87. Latches are often referred to as "one-way" or "two way." One-way latches and two-way latches are often drawn in the same manner. Mehrotra, Tr. 372, 397. Yet, they function differently. A two-way latch freely switches back and forth between two states when different input values are applied. Thus, if the input to the latch is a 0, then the value saved in the latch becomes a 0. If a subsequent input is a 1, the latch then saves a 1. However, a one-way latch is said to move in only one direction. Allen, Tr. 1077.

88. With a one-way latch, when verification occurs and the latch is set to a "1", the latch does not go back to a zero during the overall cycle of iterations. Allen Tr. 1078.

89. A one-way latch like that used in Figure 16 of the `338 patent will not allow the detection of so-called "program disturb conditions" where, due to defects in a part, a cell goes back to an erased state before the entire chunk of data is verified. Nor will a one-way latch allow the detection of conditions in which a part fails and a cell is disturbed from an erased into a programmed state. Harari, Tr. 250-252; Mehrotra Tr. 374-378; CX 2.

90. Neither claim 27 of the `338 patent, nor the specification mentions

the detection of program disturb conditions. CX 2.

91. With respect to Figure 16, the specification teaches that the output of the XOR gates passes through NOR gate 717 such that a "1" appears at the output of NOR gate 717 whenever all the bits are verified, otherwise a "0" appears there. When verification occurs (i.e. "[w]hen the control signal VERIFY is true"), "this result is latched to latch 721 such that the same result at the output of NOR gate 717 is also available at the cell compare module's output 725." CX 2 at col. 20, lines 25-32 (emphasis added). The output 725 is fed through an output line to the "program circuit with inhibit 210 of FIG. 5." CX 2 at col. 20, lines 33-36.

92. The specification in describing the functions of latch 721 states that "[w]hen the control signal VERIFY is true, this result is latched to latch 721." It says nothing about resetting latch 721 in case of a subsequent (or previous) control signal VERIFY that is not true. Thus, the specification does not provide that it will return to an unverified state during the program and verification of a chunk of data. Indeed, since latch 721 is a one-way latch, once the latch is set, the stored data cannot be affected by the output of NOR gate 717. Mehrotra, Tr. 340-341.

93. The preferred embodiment of the `338 patent is a multi-state device. If latch 721 were not a one-way latch, there would be catastrophic failure of the multi-state device. See McGreivy, Tr. 1697-1708, 1793-1813; CX 2 at col. 19, lines 4-26.

94. The specification provides that in order to change the setting of latch 721:

> At power-up or at the end of program/verify of a chunk

> of data, all cell compare module's outputs such as 725, 727 are reset to the "not verified" state of "0". This is achieved by pulling the node 726 to V_{ss} (0 V) by means of the RESET signal in line 727 to a transistor 729.

CX 2 at col. 20, lines 46-51.

95. If latch 721 were a two-way latch, before the commencement of programming a cell would be read and if found not to be in the correct state, latch 721 would flip back to the not verified state in response to the output of NOR gate 717, and it would not be necessary to reset the latch with the reset signal. Mehrotra, Tr. 399-400.

96. The specification shows that latch 721 can only be reset by the effect of transistor 729. See Mehrotra, Tr. 342. The specification demonstrates that latch 721, once set to the verified state, remains in the verified state during the entire program/verify of a chunk of data. Then, latch 721 is returned to the "not-verified" state by a reset operation in which node 726 is pulled down, as one would expect in the case of a one-way latch. See Mehrotra, Tr. 400; See also, Allen, 1079, 1086.

97. In order to pull down latch 721, one would have to design the circuit shown in Figure 16 to have transistors of the proper size. Mehrotra, Tr. 409; see also Allen Tr. 1079. The `338 patent does not indicate the size of the transistors involved in Figure 16. Nonetheless, one of ordinary skill would know how to size the transistors shown in Figure 16 relative to the size of NOR gate 717 so as to achieve a one-way latch. CX 2; Mehrotra Tr. 404-409.

98. In addition to the disclosure of Figure 16, including latch 721, Figure 5 of the '338 patent contains a block 210 entitled "Program Circuit with Inhibit." This block provides no detail regarding the

specific circuitry that actually inhibits further programming. CX 2; Guterman, Tr. 508-510.

99. Figure 17 shows "one embodiment of the program circuit with inhibit 210 of Fig. 5 in more detail." CX 2 at col. lines 52-53. The one embodiment shown in Figure 17 is relevant to the Hot Electron Injection programming method used in the preferred embodiment. The circuitry in Figure 17 is for removing voltage from the drain of a cell to inhibit further programming. CX 2, col. 20, line 52 through col. 21, line 8; Mehrotra, Tr. 352-353; Guterman, Tr. 511-513.

100. To one skilled in the art, one way of implementing the inhibit means is to combine certain disclosures in Figures 16 and 5, in particular block 190 of Figure 5, which is entitled "Read/Program Latches and Shift Register." The temporary storage latch disclosed in block 190 of Figure 5 can also serve as the inhibit latch 721 of Figure 16 of the '338 Patent. Mehrotra, Tr. 349-351; CPX 120; CX 2, Fig. 16; Pathak, Tr. 835-839; CPX 57C-58C; CPX 124-125.

101. A flash memory designer of ordinary skill would seek to combine the functions of the temporary storage latch and the verify inhibit latch in a single structure in order to save transistors, thereby reducing the surface area of the chip. Pathak, Tr. 839-840.

102. Figure 16 of the '338 patent discloses structures that correspond to the final means-plus-function element of claim 27 in a multi-state implementation. Those structures include the one-way latch 721, the outputs such as output 725, as well as AND gate 733 whose single output 735 is used to signal the controller in the preferred embodiment that all cells in the chunk of data have been correctly verified. Mehrotra, Tr. 341; CX 2 at col. 20, lines 18-51.

103. The specification provides in part: "[a]s soon as the programmed state is verified correctly, programming stops." CX 2 at col 18, lines 24-25.

104. The patent provides that "parallel programming is implemented in the preferred embodiment of the '338 Patent by a selective programming circuit which disables programming of those cells in the chunk that have already been verified correctly." CX 2 at col. 19, lines 13-16.

105. The patent also provides that "it is preferable to apply programming voltages in repetitive short pulse with a read operation occurring after each pulse to determine when it has been programmed to the desired threshold voltage level, at which time the programming terminates." CX 2 at col. 9, lines 13-18.

106. Each of the specification passages cited above clearly indicate that the '338 patent will not apply an additional programming pulse to a cell after it has been verified. See Mehrotra, Tr. 253-254; McGreivy, Tr. 1693-1696.

107. Dr. McGreivy explained that failure to terminate will, over time, overstress a binary device and make a multi-state device malfunction. McGreivy, Tr. 1697-1708, 1793-1813. This point is addressed in the text of the '338 patent, as follows:

> In the prior art EEprom devices, after each programming step, the state attained in the cell under programming is read and sent back to the controller 140 or the CPU 160 for verification with the desired state. This scheme places a heavy penalty on speed especially in view of the serial link.
>
> In the present invention, the program verification is optimized by programming a chunk (typically several bytes) of cells in parallel followed by verifying in parallel on chip. The parallel programming is implemented by a selective programming circuit which disables programming of those cells in the chunk whose states have already been verified correctly. This

feature is essential in a multi-state implementation, because some cells will reach their desired state earlier than others, and will continue pass [sic] [past] the desired state if not stopped. After the whole chunk of cells have been verified correctly, logic on chip communicates this fact to the controller, whereby programming of the next chunk of cells may commence. In this way, in between each programming step data does not need to be shuttled between the EEprom chip and the controller, and program verification speed is greatly enhanced.

CX 2 at col. 19, lines 4-26.

IV. VALIDITY

A. The '752 Patent

The Mitsuishi Patent

1. Samsung introduced United States Patent No. 4,931,997 invented by Mitsuishi (the "Mitsuishi Patent") as a potentially relevant item of prior art. RX 65.

2. The Mitsuishi Patent first embodiment limits the user to selecting either a single row or the entire chip for an erase operation. McGreivy, Tr. 1671-1673.

3. In the Mitsuishi Patent first embodiment, the contents of a protected row can be rewritten from column latches 35 into the protected row following a bulk erase of the entire chip. RX 65 at col. 4, lines 46-60, col. 7, lines 26-44, Figs. 1A and 2.

4. The Mitsuishi Patent first embodiment does not permit the selection of a plurality of rows for simultaneous erase. McGreivy, Tr. 1671-1672; RX 65 at col. 4, lines 46-60, col. 7, lines 26-44, Figs. 1A and 3.

5. The Mitsuishi Patent second embodiment bulk erases the entire chip minus the erase inhibited rows. McGreivy, Tr. 1663-1664, 1668-1670; RX 65 at col. 8, lines 23-48, Fig. 6.

6. The identity of the erase inhibited rows in the Mitsuishi Patent second embodiment is stored in row 11 of the EEprom memory array and shifted from row 11 into column latches 35 during erase operations. RX 65 at col. 8, lines 23-48, Fig. 6.

7. The Mitsuishi Patent second embodiment does not permit column latches 35 to rewrite information into row 11 of the EEprom memory array. Allen, Tr. 1154-1155; RX 65 at col. 8, lines 40-48, Fig. 6.

8. In order to change the identity of the rows selected for erase in the

Mitsuishi Patent second embodiment, the device must possess the capability of writing new information into row 11 of the EEprom memory array. Allen, Tr. 1145-1146; RX 65 at col. 8, lines 29-43, Fig. 6.

9. The Mitsuishi Patent second embodiment does not possess the capability of writing new data to row 11 of the EEprom memory array. McGreivy, Tr. 1659-1662; RX 65 at col. 8, lines 23-48, col. 10, lines 45-48, col. 11, lines 1-42, Fig. 6.

10. The Mitsuishi Patent second embodiment permanently designates a fixed group of rows of memory to be erase inhibited. McGreivy, Tr. 1655-1656, 1668-1671; Allen, Tr. 1154-1155; RX 65 at col. lines 23-48; CPX 70.

11. The Mitsuishi Patent cannot select a new plurality of rows for simultaneous erasure each time an erase operation is commenced. McGreivy, Tr. 1655-1656, 1664, 1668-1673; Allen, Tr. 1154-1155; RX 65 at col. 4, lines 46-60, col. 7, lines 26-44, col. 8, lines 23-48, col. 11, lines 8-60, Figs. 1A, 2, 6 and 11.

12. The Mitsuishi Patent does not possess a "means for selecting a plurality of sectors among the one or more chips for erase operation" as recited in claim 1 of the `752 patent. McGreivy, Tr. 1655, 1657-1673, 1675-1677, 1681-168, 1726-1727, 1729-1734, 1746, 1749-1753; Allen, Tr. 1145-1146, 1151-1155; RX 65 at col 4, lines 46-60, col. 7, lines 26-44, col. 8, lines 23-48, col. 11, lines 8-60, Figs. 1A, 2, 6 and 11.

13. The Mitsuishi Patent does not disclose the function of selecting a plurality of sectors each time an erase operation is commenced. McGreivy, Tr. 1655-1673, 1675-1677, 1681-1682, 1726-1727, 1729, 1734, 1746, 1749-1753; Allen, Tr. 1145-1146, 1151-1155; RX 65 at col. 4, lines 46-60, col. 7, lines 26-44, col. 8, lines 23-48, col. 11, lines 8-60, Figs. 1A, 2, 6 and 11.

14. There is no suggestion in the Mitsuishi Patent to combine the first and second embodiments. McGreivy, Tr. 1672-1673, 1726-1727; RX 65 at 10-11.

15. There is no suggestion in the Mitsuishi Patent that the first and second embodiment can be used simultaneously. McGreivy, Tr. 1672-167, 1726-1727; RX 65 at 10-11.

16. The first and second embodiments of the Mitsuishi Patent are incompatible and mutually exclusive. McGreivy, Tr. 1672-1673, 1726-1727.

17. The third embodiment of the Mitsuishi Patent is limited to using either the first or second embodiment, not both. The third embodiment is a single chip microcomputer for an IC card in which the EEprom of the first or the second embodiment is used. McGreivy, Tr. 1672-1673, 1726-1727; RX 65 at 10-11.

18. An individual of ordinary skill in the art would not seek to combine or merge the first and second embodiment of the Mitsuishi Patent. McGreivy, Tr. 1672-1673, 1726-1727; RX 65 at 10-11.

19. Each row of nonvolatile memory has a limited operating life. McGreivy, Tr. 1675-1677.

20. If a row from the non-volatile memory array of a EEprom chip was used to store the erase status of each row in the array, as all of the embodiments of the Mitsuishi Patent teach, the resulting device, if reconfigurable for each erase operation, would have a very limited useful life and be unusable as the EEprom system claimed in claim 1 of the '752 patent because row 11 would have to be erased and rewritten each time a new row is selected for erase. McGreivy, Tr. 1676-1677, 1751-1753.

21. An individual of ordinary skill would not design a `752 patent mass storage device that uses a row from the nonvolatile memory array to store the erase status of each row in the array. McGreivy, Tr. 1675-1677.

22. An individual of ordinary skill would not design a `752 patent mass storage device that uses the architecture of the Mitsuishi Patent second embodiment because it would be an inefficient and wasteful use of silicon. McGreivy, Tr. 1751-1753; RX 65 at 8-9.

23. The Mitsuishi Patent is practically limited to an EEprom device that uses a square array. McGreivy, Tr. 1673-1674.

24. The Mitsuishi Patent does not include an "individual register associated with each sector for holding a status to indicate whether a sector is selected or not." McGreivy, Tr. 1681-1682; Allen, Tr. 1141, 1141-1145; RX 65 at col. 8, lines 23-48, Figs. 1A, 2, 6 and 11.

25. The Mitsuishi Patent does not possess a simultaneously erasing means that is responsive to the status in each of the individual registers. McGreivy, Tr. 1681-1682; Allen, Tr. 1141-1145.

26. The Mitsuishi Patent does not possess individual registers that are simultaneously resettable to a status indicating that the associated sectors as not selected McGreivy, Tr. 1681-1682; Allen, Tr. 1141-1145.

27. The Mitsuishi Patent makes clear that the objective of its second embodiment is protecting data from illicit use. RX 65 at col. 2, lines 1-21, col. 8, lines 40-48, col. 9, line 66 - col. 10, line 14, col. 11, lines 34-41.

28. Column 3, lines 30 through column 4, lines 41 do <u>not</u> describe the operation of the Mitsuishi second embodiment as suggested by Samsung and its expert Dr. Allen. Instead, the cited text from the Mitsuishi Patent

merely describes the background EEprom technology to which the practicable embodiments of the Mitsuishi Patent will be applied. RX 65 at col. 3, line 30- col. 4, line 41.

29. Signal AS is always equal to "1" (i.e., bulk erase) in the Mitsuishi Patent's second embodiment. RX 65 at col. 8, lines 20-68.

30. Figure 6 of the Mitsuishi Patent, the most detailed disclosure regarding the structure of the patent's second embodiment, clearly shows that signal AS is not externally controlled. RX 65 at Fig. 6.

31. The first embodiment of the Mitsuishi Patent is the test mode for the device disclosed in the third embodiment of the patent. RX 65 at col. 10, lines 45-48, col. 11, lines 8-33.

32. An IC or cash card is the only application that is disclosed in the Mitsuishi Patent for the second embodiment. RX 65 at col. 10, lines 45-48, col. 11, lines 30-41.

The Bill Article

33. Samsung introduced an article authored by Colin S. Bill, et. al., entitled "A Temperature and Process-Tolerant 64K EEPROM" (the "Bill Article"), as a potentially relevant article of prior art. RX 67.

34. Dr. Allen believed that the byte described in the Bill Article was equivalent to a sector. Allen, Tr. 1164-1165.

35. In the Bill Article, the PG latch cannot be an individual register associated with each sector because it is associated with a plurality of bytes as opposed to a unique portion of the memory array. CX 1, at Fig. 3A; RX 67; Allen, Tr. 1163.

36. In the Bill Article, the disclosed device is incapable of simultaneously writing or erasing bytes into two different pages within the array. Allen, Tr. 1163; RX 67.

37. The Bill Article does not disclose the function of (or corresponding structure for) selecting a plurality of sectors. RX 67.

Cricchi Patent

38. Samsung introduced United States Patent No. 4,099,069 ("Cricchi Patent") as a potentially relevant article of prior art. RX 68.

39. The Cricchi Patent does not provide any disclosure regarding the addressing logic used to select a block of memory for erase. Allen, Tr. 1165.

40. The Cricchi Patent does not provide any structure or manner for storing the addresses of selected blocks prior to commencing the erase operation. Allen, Tr. 1165-1166.

41. The Cricchi Patent does not disclose the use of an individual register associated with each block. Allen, Tr. 1166-1168.

42. The Cricchi Patent does not provide any disclosure that the described EEprom device must be capable of storing more than one address at a time for erase operation. Thus, the Cricchi Patent does not disclose a means for selecting a plurality of sectors. Allen, Tr. 1168.

43. There is nothing in the prior art cited by Samsung that suggests that the Bill Article, the Mitsuishi Patent, the Cricchi Patent and the Sparks could be combined to build the invention claimed in the `752 patent. See RX 65, RX 66, RX 67, RX 68.

Sparks

44. Samsung introduced United States Patent No. 4,752,871 ("Sparks Patent") as a potentially relevant article of prior art. RX 66.

45. The Sparks Patent was considered by the Patent Examiner during the prosecution of the `752 patent. CX 1, "References Cited".

46. In the Sparks Patent, each EEprom subarray has its own data bus and

operates like a separate EEprom chip. RX 66 at Fig. 1.

47. In the `752 patent, all the sectors within a EEprom array share the same interface/data bus. CX 1 at Fig. 3A.

48. In the Sparks Patent, each EEprom array is completely independent of each other. The Sparks Patent permits the device to read the data from one array while simultaneously bulk erasing the data located on a separate array. RX 66 at Fig. 1.

49. LATA and LATB merely indicate what arrays are being modified by the device (programming or erasing) and should therefore be inhibited from undergoing a read operation. The setting LATA or LATB will not cause its associated array to be erased. RX 66 at Figs. 2, 3.

50. There is no disclosure in the Sparks Patent suggesting that each EEprom array should be subdivided into a plurality of sectors with each sector having an individual register for holding its erase status. RX 66 at Fig. 1.

51. Thus, the Sparks Patent does not disclose an individual register associated with each sector. RX 66 at Figs. 2.

52. In the `752 patent, all the sectors within the array are linked together, It is impossible to read one sector while erasing another. CX 1 at Fig. 3A, 4.

53. Because each array in the Sparks Patent operates like a separate chip, the Sparks Patent does not suggest the concept of dividing a single array into a plurality of individually addressable sectors. CX 1; RX 66.

54. Thus, the Sparks Patent does not disclose a means for selecting a plurality of sectors. RX 66.

Secondary Considerations of Non-Obviousness

55. The `752 patent has played a crucial role in SanDisk's success because it gives SanDisk products superior performance and endurance. Harari, Tr. 138-139.

56. Prior to 1983, no companies had used flash memory to build a solid state mass storage system. Harari, Tr. 18.

57. EEprom and other nonvolatile memory cells have a limited life time. Harari, Tr. 24-25.

58. Erasing is a very stressful process on an EEprom device. Harari, Tr. 24-25.

59. In March 1988, EEprom devices generally had a limited life of 10,0000 write-erase cycles. Harari, Tr. 25.

60. In 1988, potential solid state mass storage customers expected cell endurance to increase from 10,000 write/erase cycles to 1,000,000 cycles. Harari, Tr. 38.

61. Erase stress is reduced by having the capability of individually selecting which sectors will be erased. Harari, Tr. 38.

62. A solid state mass storage system needed a write-erase life cycle of 1 million cycles. Harari, Tr. 26-27.

63. Faster erase times were necessary before a flash EEprom device could emulate or replace magnetic hard disk drives. Harari, Tr. 31-37.

64. The term sector in the `752 patent was taken from the disk drive industry. Harari, Tr. 56.

65. Multisector erase increases the erasing speed of the EEprom device. Harari, Tr. 66-69; Mehrotra, Tr 313; Thomas, Tr. 1599-1600; CX 203.

Best Mode

66. The preferred embodiment of the `752 patent is universally applicable to all kinds of technologies and cells and was not meant to be limited to any particular memory cell or technology. Mehrotra, Tr. 319, 356-358, 389-390; CX 1 at Fig. 3A.

67. The actual circuitry or structure used to apply the erase voltage to the selected sectors depends on the type of flash memory cell being used, the cell's erase conditions, the memory architecture and the technology being used. Each technology may have its own preferred implementation. Harari, Tr. 213-214; Mehrotra, Tr. 318-320, 359-361.

68. For flash memory technologies that require a high voltage to erase a sector, [[C]]or other floating gate EEprom technologies, a dedicated voltage multiplier or a charge pump can be used to increase the voltage to the necessary level. Harari, Tr. 199-202, 212; Mehrotra, Tr. 321, 360, 410-411.

69. If a high voltage supply is available from outside of the chip, a resistor or depletion load device can be used to implement the high erase voltage necessary to erase a selected sector. Mehrotra, Tr. 360, 411.

70. For flash memory technologies that require a low or negative voltage to erase a sector, CMOS logic circuits, resistor networks, depletion load transistors or even charge pumps can be used to generate and apply the erase voltage to the selected sectors. Harari, Tr. 213-214; Mehrotra, Tr. 320-321, 411-412.

71. The methods for generating the erase voltage and applying it to a group of selected cells were well known in the art of flash memory at the time the `752 patent was filed. Mehrotra, Tr. 318-322, 359-360;

McGreivy, Tr. 1651-1652-1653.

72. One skilled in the art would know, depending on the type of technology and cell he was working with, whether to apply a resistor, charge pump or some other circuit to apply the erase voltage to the selected sectors. Mehrotra, Tr. 388; McGreivy, Tr. 1652-1653.

73. Because the inventors did not intend to limit the `752 patent to a particular cell technology, the `752 patent does not indicate a preferred method for applying the erase voltage to the selected sectors. Mehrotra, Tr. 318, 357-361, 389-390.

74. Neither Dr. Harari nor Mr. Mehrotra perceived the structure used to generate and apply the voltage to the selected sectors to be part of the inventive feature of the `752 patent. Harari, Tr. 212-214; Mehrotra, Tr. 318; CX 12 at SD072037.

75. [RESERVED]

76. Neither Dr. Harari nor Mr. Mehrotra perceived the structure used to actually generate and apply the erase voltage to the selected sectors to be part of the means for simultaneously performing the erase operation only on the plurality of selected sectors in claim 1 of the `752 patent. Harari, Tr. 201-202; Mehrotra, Tr. 392-397; CX 12 at SD072037.

77. At the time the `752 patent was filed, SanDisk was developing products which would incorporate the invention of the `752 patent. Mehrotra, Tr. 354-355.

78. For SanDisk's particular technology and desired memory specifications, SanDisk considered using a charge pump to generate the necessary voltage to accomplish erase. Mehrotra, Tr. 388-389.

79. At the time the `752 patent was filed, the inventors understood that the use of a charge pump or dedicated voltage multiplier was merely one

way of generating and applying the erase voltage to the selected sectors, but that there were other ways as well. Harari, Tr. 198-201; Mehrotra, Tr. 390-390, 410-412; CX 12 at SD072037.

80. Other techniques, such as resistors, had been used in very early Eproms and EEproms since the mid-seventies to do a similar function. Mehrotra, Tr. 388.

81. With respect to the claim element "means for simultaneously performing the erase operation on only the plurality of selected sectors" in claim 1 of the `752 patent, the emphasis of this claim is on simultaneously performing the erase operation, not how the erase voltage is generated. CX 1; see also Harari, Tr. 214-216; Mehrotra, Tr. 395-396.

82. The prior art allowed the erasure to occur to either single blocks of memory or to the entire chip. Guterman, Tr. 432-433.

83. The `752 patent addresses a solution to that problem, namely the capability to select a number of sectors which can be erased simultaneously, and the patent provides specifics on how that selection is performed. Guterman, Tr. 432-433.

Enablement and Indefiniteness

84. Given the disclosure of the `752 patent, an individual of ordinary skill in the art would understand how to make the application of an erase voltage conditional upon the output of an individual register. McGreivy, Tr. 1652.

85. Although Figure 3A depicts the erase voltage and the output of the individual registers being applied directly to the sectors, it would be obvious to any memory designer that two signals cannot be applied at the same time to a certain node and that there would have to be a means of selectively applying the voltage to the node. Mehrotra, Tr. 382-383.

86. The techniques and circuitry used for actually applying the erase voltage to the selected sectors are not part of the invention of the `752 patent. Mehrotra, Tr. 383-384, 393-397.

87. The techniques and circuitry for actually applying the erase voltage to flash memory cells were well known in the art at the time the `752 patent was filed. Mehrotra, Tr. 322.

88. One of ordinary skill in the art would know the appropriate circuits to use for a particular type of technology to actually apply the erase voltage to the sector. Mehrotra, Tr. 359, 380-381, 385-386; McGreivy, Tr. 1651-1652.

89. One of ordinary skill in the art would also understand how to generate the erase voltage necessary to erase a group of cells. McGreivy, Tr. 1652-1653.

90. One example of such circuitry would be to place a resistor between the output of the individual register associated with a sector (depicted as node 239 in Figure 3A of the `752 patent) and the output of the AND gate which contains the erase supply (also depicted in Figure 3A of the `752 patent). If the register is not tagged, the output 239 will be low, and the erase voltage will not be applied to the sector. However, if the individual register for a sector is tagged, the output 239 will be high, and the high voltage from the output of the AND gate can be applied through that same resistor to the erase electrode of the sector. Mehrotra, Tr. 386-387.

91. Another means of applying the erase voltage to the selected sectors would be a charge pump. Mehrotra, Tr. 321-322.

92. These means were well-known to flash memory designers at the time the `752 patent was filed and, a designer of ordinary skill in the art would

know, depending on the type of technology and cell he was working with, whether to apply a resistor, charge pump or some other circuit to apply the erase voltage to the selected sectors. Mehrotra, Tr. 387-388; McGreivy, Tr. 1651-1652.

93. According to Dr. Allen, a person of ordinary skill in the art that pertains to the Mitsuishi `997 patent has the same level of skill as that which pertains to the `752 patent, and provides enough information to enable a person of ordinary skill in the art to construct a EEprom system as disclosed in the `752 patent; yet, the Mitsuishi Patent does not disclose any circuit mechanism for generating an erase voltage. Allen, Tr. 1135-1136.

94. [RESERVED]

95. [RESERVED]

96. Samsung's expert, Dr. Allen, admitted that the `752 patent is a logic level disclosure. Allen, Tr. 1003-1004, 1122.

97. Dr. Allen admitted that one of ordinary skill in the art of the `752 patent would know to use AND circuitry to connect the two signals coming into the sector selected for erase. Allen, Tr. 1123-1125, 1128-1129.

B. The `338 Patent

Anticipation

The M293

98. Samsung introduced an M293B1 television tuner device manufactured by SGS Thomson ("the M293") as a potentially relevant item of prior art. RX 309.

99. The M293 does not perform the function of permanently "inhibiting the programming of correctly verified cells until all the plurality of addressed cells are verified correctly" as required by the last element

of claim 27. McGreivy, Tr. 1691-1693, 1793-1794; RT 1818, 1830-1831, 1843; RX 180 at 12-13 and Exh. 1, Sheet 7; CPX 73; CX 199; RX 71.

100. The M293 permits the application of additional programming pulses to an already verified cell. McGreivy, Tr. 1691-1693, 1793-1794; Mehrotra, Tr. 1818, 1830-1831, 1843; Gross, Tr. 1453-1454; RX 180. at 12-13 and Exh. 1, Sheet 7; CPX 73; CX 199; RX 71.

101. The M293 "conditionally" or "temporarily" inhibits the programming of verified cells on a pulse-by-pulse basis. Gross, Tr. 1453-1454; RX 180 at 12-13 and Exh. 1, Sheet 7; McGreivy, Tr. 1691-1693, 1793-1794; Mehrotra, Tr. 1818, 1830-1831, 1843; CPX 73; CX 199; RX 71; CPX 73; CX 199.

102. The M293 does not possess any structure that is capable of permanently inhibiting the programming of correctly verified cells. Allen, Tr. 1115; RPX 43; RX 180, at 12-13, Exh. 1, Sheet 7; McGreivy, Tr. 1687-1690, 1691, 1787-1788; CX 199.

103. The M293 device does not possess the one-way latch that is disclosed in circuit 721 of Figure 16 of the `338 patent. Allen, Tr. 1115; RPX 43, RX 180, at 12-13, Exh. 1, Sheet 7; CX 2, at Fig. 16.

104. The "temporary" or "conditional" inhibit present in the M293 would not function for a multistate device. McGreivy, Tr. 1699-1701.

105. The permanent inhibition of verified cells disclosed in the `338 patent is critical to the successful operation of multistate devices. McGreivy, Tr. 1699-1701, 1706.

106. The element in claim 27 which requires permanently inhibiting the programming of verified cells is beneficial to binary NAND devices. Harari, Tr. 73, 1863-1865, 1867-1868; Choi, Tr. 1409.

107. CX 204 is a true and correct copy of a report entitled "An Analysis of

SGS Thomson M293B1 EPM32: Electronic Program Memory for 32 Stations" that was prepared by Chipworks, Inc. ("Chipworks Report"). CX 204.

108. The Chipworks Report is an analysis of the SGS Thomson M293 device that was jointly commissioned by SanDisk and Samsung. CX 204, cover page.

109. The Chipworks Report was the result of extensive reverse engineering analysis of relevant internal circuits of the M293. CX 204 at 1.

110. The Chipworks reverse engineering analysis included a review of the following documentation: (1) the TAEUS Technology Analysis Report entitled "SGS M293 Electronic Program Memory Device ("TAEUS Report") (RX 180C); (2) M293 Data Sheet (RX 98); (3) SGS Technical Note 153 (RX 96); and (4) an article by Guido Torelli entitled "An Improved Method For Programming A Word-Erasable EEPROM" ("Torelli Article"). CX 204 at Tabs 5-8.

111. The Chipworks reverse engineering analysis included removal of the plastic package surrounding the chip and photographing of the relevant circuits. CX 204 at 12, Tab 2.

112. The Chipworks analysis included the microprobing of the internal bit lines of the M293 in order to observe the voltage waveforms during programming and read cycles. CX 204 at 12.

113. In order to microprobe, it was necessary for Chipworks to (1) jet etch a hole through the plastic package to expose the die and (2) remove the scratch protection layer by a wet acid etch to allow direct contact to the metal interconnect lines. CX 204 at 12.

114. The test jig used by Chipworks to test the M293 was constructed around a 28-pin ZIF socket to hold the M293 during the test. CX 204 at 12.

115. In the morning test session of October 15, 1996, the probe tip used to

contact a bit line was connected to a Tektronix TDS380 digital real time oscilloscope via a 10x attenuating probe having an impedance of 14.1 pF and 10 Megaohms. CX 204.

116. In the afternoon test session of October 15, 1996, the oscilloscope was changed to a Tek TDS700A series unit with a 10x attenuating probe of higher impedance: 8.0pF and 10 Megaohms. CX 204.

117. A single M293 device was used for all measurements. CX 204 at 13.

118. Only one bit line was probed for any given measurement depicted in the waveforms attached to Tab 4 of the Chipworks Report. CX 204 at 13, Tab 4.

119. Electrical tests and measurements were made on 6 arbitrary bit lines. CX 204 at 13.

120. All electrical measurements were made at room temperature. CX 204 at 13.

121. The electrical test measurements were made in a semi-darkened room to reduce the light striking the die to a very low level. CX 204 at 13.

122. The test procedures used by Chipworks were agreed to by both SanDisk and Samsung.

123. Both SanDisk and Samsung had representatives present when Chipworks performed the electrical testing.

124. The Chipworks Report confirms the testimony of Dr. Allen and Dr. McGreivy that the M293 does not possess a structure to permanently inhibit programming. Allen, Tr. 1115; McGreivy, Tr. 1687-1690, 1691, 1787-1788.

125. In the M293, the programming of the selected cell on each column of the array is done by applying a sequence of high voltage programming pulses ("Vpp"). CX 204 at 4.

126. During programming, each individual programming pulse to a cell in the M293 device is followed by a verify read operation. CX 204 at 4.

127. When the M293 is in programming mode, the result of the verify read is retained only until the time of the next potential programming pulse. CX 204 at 4.

128. The verify read of the M293 only controls the application or inhibit of a single programming pulse. CX 204 at 4.

129. Programming in the M293 device stops when only all the cells are verified. The M293 does not possess any structure for permanently inhibiting the programming of correctly verified cells. CX 204 at Fig. A.

130. The M293 does not possess a structure to generate a program "lock-out" signal that will guarantee that no further programming will occur once a verify read operation reads a "1" (i.e., the cell has achieved its target programming state) for the first time. CX 204 at 4.

131. The M293 does not possess any structure to guarantee that no further programming will occur to a cell after a verify read operation reads a "1" for the first time. CX 204 at 4.

132. In the M293, it is possible that after one programming pulse has been inhibited, a subsequent pulse will be allowed on the previously verified and inhibited cell. CX 204 at 4.

133. The M293 stops programming altogether when the verify read operation results in "all one" being read across all bits (cells) of the selected word. CX 204 at 4.

134. The results of the Chipworks Report (the M293 does not permanently inhibit) is fully consistent with the results of (1) the SanDisk test report of the M293 and M296 (CX 199) and (2) TAEUS Report (RX 180C).

Compare CX 204 with CX 199 and RX 180C.

135. The application of an additional programming pulse to an M293 cell that has already been verified is possible if the cell has been programmed into a voltage region which produces a sense amplifier misread. CX 204 at 5-6.

136. The M293 uses a sense amplifier to "read" the state of the cell to determine whether a cell being programmed has achieved the "1" or programmed state. CX 204 at 2, 5-6.

137. Any sense amplifier has a small region of input voltages where the resulting output is uncertain and a misread is possible. CX 204 at 5-6.

138. During programming operations, the M293 applies a programming pulse whenever the cell being programmed reads a "0". CX 204 at 9.

139. In the M293, for those cells that read as a "1" (or the "programmed" state), the programming inhibit circuit prevents programming transistor T1 from being turned on and applying a high voltage to the cell. CX 204 at 2-3, 7, 9.

140. The electrical tests of the M293 conclusively show that the M293 does not possess a lock out that guarantees that additional programming pulses will not be applied to a cell after it has been verified. CX 204 at Tab 4.

141. Each and every waveform generated for the Chipworks Report show that the M293 can apply an additional programming pulse to a cell that has been previously inhibited. CX 204 at Tab 4.

142. The capacitive loading of the testing equipment used by Chipworks could cause a misread of an "almost 1" cell as a "1" subsequent to the programming pulse. CX 204 at 9.

143. The misread of an "almost 1" cell is immaterial to the Chipworks

analysis because it does not affect the conclusion that the M293 does not possess any structure for permanently inhibiting the programming of verified cells. CX 204 at 4

144. For an "almost 1" cell that is incorrectly inhibited from programming, the inhibiting of the programming pulse eliminates the high voltage charge on the loaded bit line to bias the next verify read and allows the cell to be correctly read as a "zero." CX 204 at 9.

145. Using the Chipworks test set-up for the M293, if a cell is inhibited for two or more programming pulses, the application of an additional programming pulse cannot be attributed to the capacitive loading of the test set-up. CX 204 at 9.

146. Using the Chipworks test equipment and set-up for the M293, an electrical test where a cell is inhibited for two consecutive pulses and then has a high voltage applied to it during the application of the third programming pulse necessarily indicates that the cell had been programmed into a region where the sense amplifier read result is uncertain. CX 204 at 10.

147. Tab 4, Trace 10 of the Chipworks Report shows a programming cycle where the M293 inhibited the cell being measured for two consecutive programming pulses before applying an additional programming pulse. CX 204 at 10, Tab 4, Trace 10.

148. Tab 4, Trace 10 of the Chipworks Report shows an electrical waveform that was made under test conditions where the high voltage pulse Vpp was set to 23 volts. A Vpp of 23 volts is 1 volt under the data book specifications. CX 204 at 10, Tab 4, Trace 10; RX 98.

149. Tab 4, Trace 10 of the Chipworks Report shows that after inhibiting two consecutive pulses, the M293 applied an additional programming pulse

to the cell. CX 204 at 10, Tab 4, Trace 10.

150. Tab 4, Trace 12 of the Chipworks Report shows an electrical waveform that was made under test conditions where the high voltage pulse Vpp was set to 24 volts. CX 204 at 10, Tab 4, Trace 12.

151. A high voltage Vpp of 24 volts is within the parameters recommended by the M293 data book. RX 98.

152. Tab 4, Trace 12 of the Chipworks Report shows a programming cycle where the M293 inhibited the cell being measured for two consecutive programming pulses before applying an additional programming pulse. CX 204 at 10, Tab 4, Trace 12.

The Torelli Article

153. Samsung introduced an article authored by Guido Torelli, et. al., entitled "An Improved method for programming a word-erasable EEPROM" (the "Torelli Article"), as a potentially relevant article of prior art. RX 71.

154. The Torelli Article described the operation and characteristics of the M293 device. Allen, Tr. 1044-1046.

155. The Torelli Article does not disclose the function of permanently inhibiting the programming of correctly verified cells. Allen, Tr. 1175-1177; McGreivy, Tr. 1687-1690; RX 71 at 490 and Fig. 4; CPX 73.

156. The Torelli Article does not suggest to an individual of ordinary skill in the art the function of permanently inhibiting the programming of correctly verified cells. Allen, Tr. 1175-1177; McGreivy, Tr. 1687-1690; RX at 490 and Fig. 4; CPX 73.

157. The Torelli Article, specifically Figure 4, indicates that the cells being programmed are verified between each and every programming pulse. McGreivy, Tr. 1687-1690; CX 86, at Fig. 4; CPX 73.

158. At most, the Torelli Article, specifically Figure 4, discloses a device that conditionally inhibits the programming of cells on a pulse-by-pulse basis. McGreivy, Tr. 1687-1690; CX 86 at Fig. 4; CPX 73.

159. The Torelli Article does not disclose any structure that is capable of permanently inhibiting the programing of correctly verified cells. Allen, Tr. 1038, 1192; McGreivy, Tr. 1689; RX 71 at Fig. 2.

160. The Torelli Article does not disclose any structure, like a one-way latch, that is capable of remembering whether a cell has been previously verified and inhibited during the application of previous programming pulses. Allen, Tr. 1038, 1192; McGreivy, Tr. 1689; RX 71 at Fig. 2.

161. The Torelli Article does not disclose any structure for temporarily storing a chunk of data for programming a plurality of addressed cells. Allen, Tr. 1020, 1191; McGreivy, Tr. 1759; RX 71 at Fig. 2.

162. The Torelli Article does not indicate whether the temporarily stored data is to be stored on or off chip. McGreivy, Tr. 1759, 1762; RX 71 at Fig. 2.

163. The Torelli Article does not disclose any structure for verifying the programmed data in each of the plurality of addressed cells with a chunk of stored data. Allen, Tr. 1034, 1191-1192; RX 71 at Fig. 2.

164. The Torelli Article does not disclose any structure for inhibiting programming of correctly verified cells among the plurality of addressed cells. Allen, Tr. 1038, 1192; McGreivy, Tr. 1686; RX 71 at Fig. 2.

165. The Torelli Article does not disclose any structure for further programming and verifying in parallel the plurality of addressed cells and inhibiting the programming of correctly verified cells until all the plurality of addressed cells are verified correctly. McGreivy, Tr. 1686-1691, 1784; RX 71 at Fig. 2.

166. The failure of the Torelli Article to disclose a structure for (1) "temporarily storing a chunk of data for programming a plurality of addressed cells"; (2) "verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data"; (3) "inhibiting further programming of correctly verified cells among the plurality of addressed cells"; and (4) "further programming and verifying in parallel the plurality of addressed cells and inhibiting the programming of correctly verified cells until all the plurality of addressed cells are verified correctly", would preclude an individual of ordinary skill from building the device disclosed in claim 27 of the `338 patent. McGreivy, Tr. 1685, 1787-1788.

Obviousness

167. An individual of ordinary skill in the art of flash memory design and development has a working knowledge of digital logic. McGreivy, Tr. 1650.

168. A working knowledge of digital logic is obtained by someone working probably about two years in the field of integrated circuit design. McGreivy, Tr. 1651.

169. The skill level of an individual with a working knowledge of digital logic is comparable to a bachelor's level degree and some work experience in the field of integrated circuit design. McGreivy, Tr. 1651. Respondents' expert, Dr. Allen, also testified that the level of ordinary skill in the art pertaining to the `338 patent is a bachelor's degree in electrical or computer engineering, an understanding of digital design, computer architecture, and flash EEPROM cell technology, and a few years of work experience in flash EEPROM technology. See RPFF 56; Allen, Tr. at 1007.

170. Individuals of ordinary skill in the art of flash memory design and development have an understanding of integrated circuit fabrication, so that they understand the design rules and circuitry provided by wafer manufacturers. McGreivy, Tr. 1650-1653.

171. An individual of ordinary skill in the art of flash memory design and development has knowledged of semiconductor testing. McGreivy, Tr. 1650.

172. An individual of ordinary skill in the art of flash memory design and development understands device specifications. McGreivy, Tr. 1650.

173. The level of ordinary skill in the art of flash memory design and development is the same for both the `338 and `752 patent. McGreivy, Tr. 1650-1651.

174. Samsung introduced as potentially relevant items of prior art excerpts from a 1993 SGS Thomson Data Book which pertained to the following devices: the M193A, M193C, M193D, M206, M293, M490 and M491 (the "M193A Data Book," "M193C Data Book," "M206 Data Book," "M293 Data Book," "M490 Data Book," and "M491 Data Book" respectively). RX 91-100.

175. The M293 Databook does not disclose the function of permanently inhibiting the programming of correctly verified cells. RX 98 at SEC39804-05; McGreivy, Tr. 1691, 1687-1690, 1787-1788.

176. The M206 Data Book does not disclose the function of permanently inhibiting the programming of correctly verified cells. RX 100, at SEC39852; McGreivy, Tr. 1691, 11887-1690, 1787-1788.

177. The M490 and M491 Data Books do not disclose the function of permanently inhibiting the programming of correctly verified cells. RX 99, at SEC39820-21; McGreivy, Tr. 1687-1691, 1787-1788.

178. The M293, M206, M490 and M491 Data Books combined do not disclose the

function of permanently inhibiting the programming of correctly verified cells. McGreivy, Tr. 1691, 1787-1788; CPX 73.

179. The M293 Data Book does not suggest the function of permanently inhibiting the programming of correctly verified cells. RX 98 at SEC39804-05; McGreivy Tr. 1687-1691, 1787-1788.

180. The M206 Data Book does not suggest the function of permanently inhibiting the programming of correctly verified cells. RX 100 at SEC39852; McGreivy, Tr. 1687-1691, 1787-1788.

181. The M490 and M491 Data Books do not suggest the function of permanently inhibiting the programming of correctly verified cells. RX 99 at SEC39820-21; McGreivy, Tr. 1687-1691, 1787-1788.

182. The M293, M206, M490 and M491 Data Books combined do not suggest to an individual of ordinary skill in the art the function of permanently inhibiting the programming of correctly verified cells. McGreivy, Tr. 1687-1691, 1787-1788; RX 98, at SEC39804-05; RX 100, at SEC39852; RX 99, at SEC39820-21.

183. Samsung introduced the SGS Technical Note 152 ("Technical Note 152"), authored by Guido Torelli et. al. in 1982, as a potentially relevant item of prior art. RX 95.

184. Technical Note 152 does not disclose or suggest the function of permanently inhibiting the programming of correctly verified cells. RX 95, at 39736.

185. Samsung introduced the SGS Technical Note 153 ("Technical Note 153"), authored by Guido Torelli et. al. in 1982, as a potentially relevant item of prior art. RX 95.

186. Technical Note 153 does not disclose or suggest the function of permanently inhibiting the programming of correctly verified cells. RX

96, at SEC39754.

187. Samsung introduced the SGS Technical Note 170 ("Technical Note 170"), authored by Guido Torelli et. al. in 1984, as a potentially relevant item of prior art. RX 95.

188. Technical Note 170 does not disclose or suggest the function of permanently inhibiting the programming of correctly verified cells. RX 94, at SEC39774-75.

189. Technical Notes 152, 153 and 170 combined do not disclose the function of permanently inhibiting the programming of correctly verified cells. RX 95, at 39736; RX 96, at SEC39754; RX 94, at SEC39774-75.

190. There is no suggestion in the Torelli Article, M293, M206, M490 and M491 Data books or Technical Notes 152, 153 and 170 that these pieces of art should be combined together to build the invention claimed in claim 27 of the `338 patent. McGreivy, Tr. 1787-1788; RX 71, 94-96, 98-100.

191. The record is devoid of any evidence to suggest that an individual of ordinary skill would have attempted to combine the Torelli Article, M293, M206, M490 and M491 Data books or Technical Notes 152, 153 and 170 to build the invention claimed in claim 27 of the `338 patent. See McGreivy, Tr. 1685, 1787-1788; RX 71, 94-96, 98-100.

192. Dr. Allen, Samsung's validity expert, offered no testimony to suggest that one would know how to combine the Torelli article, SGS data books and SGS technical notes. See Allen, Tr. 1004-1195.

193. In combination, the Torelli Article, M293, M206, M490 and M491 Data books or SGS Technical Notes 152, 153 and 170 do not suggest to an individual of ordinary skill in the art the function of permanently inhibiting the programming of correctly verified cells. McGreivy, Tr. 1685, 1687-1690, 1787-1788; RX 71 at 490 and Fig. 4; CPX 73; RX 98, at

SEC39804-05; RX 99, at SEC39820-21; RX 100, at SEC39852; RX 95, at 39736; RX 96, at SEC39754; RX 94, at SEC39774-75.

194. In combination, the Torelli Article, M293, M206, M490 and M491 Data books or Technical Notes 152, 153 and 170 do not disclose any structure for inhibiting programming of correctly verified cells among the plurality of addressed cells. Allen, Tr. 1038, 1192; McGreivy, Tr. 1686, 1784; RX 98 at SEC39804-05; RX 99 at SEC39820-21; RX 100 at SEC39852; RX 95 at 39736; RX 96 at SEC39754; RX 94 at SEC39774-75.

195. In combination, the Torelli Article, M293, M206, M490 and M491 Data books or Technical Notes 152, 153 and 170 do not disclose any structure for further programming and verifying in parallel the plurality of addressed cells and inhibiting the programming of correctly verified cells until all the plurality of addressed cells are verified correctly. Allen, Tr. 1038, 1192; McGreivy, Tr. 1686, 1784; RX 98, at SEC39804-05; RX 99, at SEC39820-21; RX 100, at SEC39852; RX 95, at 39736; RX 96, at SEC39754; RX 94, at SEC39774-75.

196. The Torelli Article does not render obvious claim 27 of the `338 patent. See, e.g., McGreivy, Tr. 1685, 1687-1690, 1787-1788; RX 71.

197. The Torelli Article in combination with the SGS data books and technical notes does not render obvious claim 27 of the `338 patent. McGreivy, Tr. 1685, 1687-1690, 1787-1788 RX 71; RX 98 at SEC39804-05; RX 99, at SEC39820-21; RX 100, at SEC39852; RX 95, at 39736; RX 96, at SEC39754; RX 94, at SEC39774-75.

198. The function of permanently inhibiting the programming of correctly verified cells would not be obvious to an individual of ordinary skill in the art. Harari, Tr. 1863-1865, 1867-1868.

199. Toshiba, the original designer of the NAND architecture, did not

include a permanent inhibit feature in its original 4Mbit memory product. Harari, Tr. 1863-186.

200. The `338 patent has been and will be crucial to SanDisk's success in the mass storage flash memory market. Harari, Tr. 139-140.

201. Intel Corporation, the world's largest commodity flash memory producer, entered into a licensing agreement for all of SanDisk's patents, including the `752 and `338 patents. CX 115; Harari, Tr. 128-120, 281.

202. Intel Corporation acknowledged that a fair and reasonable royalty for SanDisk patents is [[C]] percent in cash and services, with a cap on payments of $[[C]]per quarter. CX 115 at 8; Harari, Tr. 282-287.

203. In 1994, SanDisk was the worldwide leader in the mass storage flash memory with approximately a 40% market share. Harari, Tr. 138-140.

204. Programming is a very stressful process that reduces the life of an EEprom device. Harari, Tr. 24-25.

205. Dr. McGreivy believed that a misverify could "easily" occur in the M293 device. McGreivy, Tr. 1796.

206. Dr. McGreivy agreed that because precision was not essential for a TV tuner the inability of the M293 to permanently inhibit the programming of correctly verified cells did not prevent the M293 from providing satisfactory performance. McGreivy, Tr. 1802.

207. There is no explicit reference to the M293 device in the Torelli Article. RX 71.

208. There is no structure disclosed in the Torelli Article that would indicate what was meant by the term bit-per-bit intelligent writing. McGreivy, Tr. 1684-1685.

209. Torelli left it to the reader to infer what bit-per-bit intelligent writing meant. McGreivy, Tr. 1684-1685, 1768-1770.

210. The capacitance of the microprobe used to test the M293 device had no impact on the conclusions of the SanDisk test report because the M293 does not have any structure to terminate the programming of correctly verified cells. Mehrotra, Tr. 1835.

211. As Dr. McGreivy testified at the hearing, the deposition response he gave on July 31, 1996 assumed that the individual of ordinary skill in the art had in his or her possession an M293 part to generate a circuit schematics of the part through reverse engineering. Dr. McGreivy's deposition answer was never meant to be applied to a situation where the individual only had the Torelli Article and SGS Public literature in his or her possession. McGreivy, Tr. 1787-1790.

212. The SGS data book and technical notes disclose only the recommended voltage conditions. RX 94, RX 95, RX 96, RX 97, RX 98, RX 99.

213. The capacitance of the microprobe used to test the M293 device had no impact on the conclusions of the SanDisk test report because the M293 does not have any structure to terminate the programming of correctly verified cells. Mehrotra, Tr. 1835.

214. Claim 27 of the `338 patent does not make any reference to the use of reference cells during a programming operation on the plurality of addressed cells. CX 2 at 26.

215. In the `338 patent, the verification of a cell is a one-time event. A cell can be "correctly verified" only once during a given programming operation on the chunk of addressed cells. Mehrotra, Tr. 253-254; CX 2 at col. 18, line 1 - col. 19, line 16.

216. The specification of the `338 patent clearly states that disclosed

EEprom device disables the programming of all the cells that have been verified. CX 2 at 19.

217. Dr. McGreivy testified that the following portions of the `338 patent specifications formed in part the basis for his opinion that the last element of claim 27 mandated that the device permanently inhibits the programming of correctly verified cells: column 9, lines 5-17; column 18, lines 17-29; and column 19, lines 10-26. McGreivy, Tr. 1693-1696.

218. As Dr. McGreivy testified, terminating the programming of cells upon verification is an essential feature of multistate device. McGreivy, Tr. 1699-1701, 1706.

219. Dr. McGreivy testified that an EEprom device will experience greater stress and reduced life if programming of cells is not terminated upon verification. McGreivy, Tr. 1699, 1797-1798.

220. Samsung failed to put forth any type of documentary evidence in support of its claim that termination is not an important feature in a multistate device. Allen, Tr. 999-1195.

221. The purpose of the permanent inhibit feature claimed in claim 27 of the `338 patent is to prevent the application of a programming pulse to a cell that has been verified. McGreivy, Tr. 1699-1701, 1706, 1797-1798.

222. In the `338 patent, the verification of a cell is a one-time event. A cell can be "correctly verified" only once during a given programming operation on the chunk of addressed cells. Mehrotra, Tr. 253-254; CX 2 at 18-19.

223. The specification of the `338 patent clearly states that the disclosed EEprom device disables the programming of all the cells that have been verified. CX 2 at 19.

224. Claim 27 of the `338 patent does not make any reference to the use of reference cells during a programming operation on the plurality of addressed cells. CX 2 at 26.

225. As Dr. Harari testified, the permanent inhibit feature of claim 27 would enable a binary device to save power. Harari, Tr. 1864-1865, 1867-1868.

226. Toshiba's NAND products in 1990 and 1991 did not possess a means for terminating programming to correctly verified cells. In 1992, Toshiba's products for the first time contained the termination feature. Harari, Tr. 1867-1868.

V. **INFRINGEMENT**

The '752 Patent

Infringement by Devices with Samsung's Original Designs

1. Samsung's 16 Mbit and 32 Mbit flash memory devices (before design change) operate in substantially the same way with respect to their implementation of the '752 patent. See Pathak, Tr. 679, 722.

2. SanDisk does not maintain that Samsung's 4 Mbit devices incorporate the multiblock erase feature. CPFF 147; Tr. 1221 (counsel); RX 154C at 2.

3. Samsung's flash memory devices (before design change) perform multiblock erase. CX 193C (Ali Dep.) at 185-186.

4. Samsung's corporate representative, Y. J. Choi, and its expert, Mammen Thomas, both testified that Samsung's first generation 16 Mbit devices (after design change) are capable of performing multiblock erase using the Pathak Sequence. CX 202C (Choi) at 440-441; Thomas, Tr. 1601-1602.

5. [[C]] Choi, Tr. 1399-1401.

6. [[C]] CX 193C (Ali Dep.) at 474-475.

7. [[C]] Choi, Tr. 1425-1426; CX 151C.

8. [[C]] CX 193C (Ali Dep.) at 156-157.

9. [[C]

] CX 193C (Ali Dep.) at 160.

10. [[C]

] CX 193C (Ali Dep.) at 205-206.

11. Toshiba has manufactured and marketed flash memory products which contain a multiblock erase feature. CX 193C (Ali Dep.) at 220-221.

12. National Semiconductor has marketed flash memory products which contain a multiblock erase feature. CX 193C (Ali Dep.) at 225.

13. Samsung's marketing people promoted its multiblock erase feature as providing "higher performance" and listed the feature as one of the reasons why its flash memory products were "the ideal solution" for mass storage applications. CX 193C (Ali Dep.) at 436, 440-444; CX 143C at SEC019927, SEC019930; CX 150 (Samsung marketing foils) at 23174, 23192; CX 178 (Samsung marketing foils) at 18065; CX 179 (Samsung seminar foils) at 17832, 17841.

14. [[C]

]

CX 193C (Ali Dep.) at 468.

15. M-Systems had a small application which utilized the multiblock erase feature in Samsung's flash memory products. CX 193C (Ali Dep.) at 468.

16. [[C]

] CX 193C (Ali Dep.) at 481-482.

17. [[C]

] CPX 105C.

18. [[C]

] CX 111C; CX 112C.

19. [[C]

] CX 151C.

20. Samsung's data books and marketing literature describe the multiblock erase capabilities of Samsung's 16 Mbit, 32 Mbit and 64 Mbit flash memory devices (before design change). CX 28 at 11234.

21. Samsung's flash memory devices with the "original designs" (i.e., 16 Mbit and 32 Mbit devices (before design change) and first generation 16 Mbit devices (after design change)) contain each and every element of claims 1, 2 and 4 of the `752 patent. See Pathak, Tr. 679.

22. Mr. Thomas, Samsung's expert, did not offer any opinion as to whether Samsung's flash memory circuits with the original designs infringe the `752 patent. Thomas, Tr. 1602-1603; RPX 61D.

23. Samsung's flash memory devices possess one or more integrated circuit chips each having an array of Flash EEprom cells partitioned into a plurality of sectors, each sector addressable for erase such that all cells therein are erasable simultaneously. Pathak, Tr. 723.

24. [[C]

] Pathak, Tr. 724-726; CX 28 at 11235.

25. [ ] Pathak, Tr. 728; CX 28 at 11235.

26. [[C]] Pathak, Tr. 726;

CX 28 at 11235.

27. [[C]] Pathak, Tr. 724-726; CX 28.

28. [[C]] Pathak, Tr. 726; CX 28 at 11235.

29. [[C]] Pathak, Tr. 726.

30. [ ] Pathak, Tr. 726-727; CX 28 at 11247.

31. Samsung's flash devices with the original designs also possess a "means for selecting a plurality of sectors" and an "individual register" as disclosed in the patent. Pathak, Tr. 730, 734-735.

32. [[C]] Pathak, Tr. 730-735; CX 46C; CPX 63C.

33. [[C]]. Pathak, Tr. 737-739; CX 48C.

34. [[C]] Pathak, Tr. 730-734; CX 46C; CPX 63C.

35. [[C]] Pathak, Tr. 743-744; CX 29 at 35367.

36. [[C]] See

Pathak, Tr. 749-750.

37. [[C]

] Pathak, Tr. 735-737, 785-786; CX 28 at 11247; CX 46C; CPX 63C.

38. [[C]

]

Pathak, Tr. 733; CX 28 at 11247; CX 46C.

39. [[C]

] Pathak, Tr. 728, 782; CX 28.

40. Samsung's devices with the original designs possess structures which correspond to the "means for simultaneously performing erase operation on only the plurality of selected sectors" disclosed in claim 1 of the `752 patent. Pathak, Tr. 727-728, 782-783; CX 28 at 11247; CPX 63C.

41. [[C]

] Pathak, Tr. 783.

42. Samsung's devices are often sold in the United States with a controller. Harari, Tr. 143-146; RX 184; CPX 106.

43. Samsung's flash memory devices have few uses without a controller. Harari, Tr. 45-49, 110-113, 137, 144-145, 177-179, 184-187; Mehrotra, Tr. 362-365; Pathak, Tr. 911; McGreivy, Tr. 1756-1757; CPX 106. See Choi, Tr. 1343-1344.

44. Samsung's flash devices with the original designs practice claim 2 of the `752 patent, which recites that "the simultaneously erasing means is

responsive . . . such that only the selected sectors are included in the erasing." Pathak, Tr. 785-786.

45. Samsung's devices with the original designs practice claim 4 of the '752 Patent. See Pathak, Tr. 786-787; CPX 63C.

46. [[C]] Pathak, Tr. 786-787.

47. [[C]] Pathak, Tr. 786-787.

48. [[C]] Pathak, Tr. 750-754; CX 28 at 11247.

49. [[C]

]

Pathak, Tr. 754-760; CX 50C at 21556.

50. [[C]

] Pathak, Tr. 754-760.

51. [[C]

] Pathak, Tr. 770.

52. [[C]

] Pathak, Tr. 771-772.

53. [[C]

] Pathak, Tr. 754-760.

54. [[C]

] Pathak, Tr. 754-760, 761-772; CX 63C; CX 64C.

55. [[C]

] Pathak, Tr. 761-772; CX 63C; CX 64C.

56. [[C]] Pathak, Tr. 770.

57. [[C]

] Pathak, Tr. 768-771.

58. [[C]

] Pathak, Tr. 760-761; CX 170C.

59. [[C]

] Pathak, Tr. 768-772.

60. [[C]

] Pathak, Tr. 760-761; CX 170C.

61. The ability of Samsung's first generation 16 Mbit devices (after design change) to perform multiblock erase through issuance of this command sequence has been confirmed by testing and/or simulation performed by both parties. Pathak, Tr. 776-777; CX 170C; CX 202C (Choi Dep.) at 440-441.

62. Samsung's expert Mammen Thomas and its design engineer Y. J. Choi testified that they did not believe that Samsung's devices could perform multiblock erase before the Pathak Sequence was identified by SanDisk's expert. Thomas, Tr. 1548, 1551; RX 15; Choi, Tr. 1405.

63. According to Samsung's own data book, [[C]

] Pathak, Tr. 774-775; CX 28 at 11240.

64. [[C]

] Pathak, Tr. 777, 994-995; CX 170C.

65. Commercial controllers are capable of issuing commands at a rate of two commands every 80 nanoseconds or faster. Pathak, Tr. 777-779.

66. Nothing would prevent Samsung from releasing a data book which set

forth the Pathak Sequence. Thomas, Tr. 1552-1553.

67. Samsung's first generation flash memory devices (after design change) infringe claims 1, 2 and 4 of the '752 patent. See FF V 1-66.

68. [[C]]

Choi, Tr. 1399-1400.

69. [[C]

] CX 29 (Samsung 1996 Data Book) at 60.

70. [[C]

] CX 29 (Samsung 1996 Data Book) at 60.

71. [[C]

] CX 29 (Samsung 1996 Data Book) at 62; Pathak, Tr. 996-997.

72. [[C]

] CX 29 (Samsung 1996 Data Book at 60, 62, 63; Pathak, Tr. 996-997.

73. [[C]

] Pathak, Tr. 774-775; CX 29 (Samsung 1996 Data Book) at 63.

74. [[C]

] Pathak, Tr. 774-775; CX 29 (Samsung 1996 Data Book) at 63.

75. [[C]

] Pathak, Tr. 774-775, 781; CX 29 (Samsung 1996 Data Book) at 63.

76. [[C]

] Pathak, Tr. 762-775, 781; CX 63C (hspice simulations); CX 64C (simulation schematic).

77. [[C]] Pathak, Tr. 772-775, 781.

78. [[C]

]Pathak, Tr. 762-775, 781; CX 63C (hspice simulations); CX 64C (simulation schematic).

79. [[C]

] Pathak, Tr. 777.

80. Samsung's expert, Joel Karp, did not test other than Samsung's second generation 16 Mbit, 32 Mbit and 64 Mbit devices (after design change) to determine whether they are capable of performing multiblock erase. Karp, Tr. 1622-1624.

81. [

] Choi, Tr. 1419-1421.

82. A TDK flash memory card, which utilizes Samsung flash memory chips with a controller was admitted into evidence. CPX 106; Harari, Tr. 144-145.

New Designs

83. Complex flash memory chips similar in complexity to the Samsung 16M NAND Flash Memory Device cannot be designed without using a computer data base. Pathak, Tr. 703-706.

84. The analysis of Samsung's flash memory circuits and designs takes an enormous amount of time and effort on the order of six man years. Thomas, Tr. 1546.

85. To understand complex flash memory circuits fully, an individual needs a list of the signals in the device and the function for each of these signals. Pathak, Tr. 705-706.

86. A computer circuit data base enables an individual to track each and every signal and determine how the signal is connected. Pathak, Tr. 706.

87. An internal signal list contains a description of each signal used in a flash memory device. Pathak, Tr. 986-990; CX 44C at SEC12848, SEC12852, SEC12854; CPX 63C.

88. [[C]

] Pathak, Tr. 754-760, 986-992.

89. An internal signal diagram illustrates how signals in the flash memory device are generated, interact and behave. Pathak, Tr. 990-991; CX 44C at SEC12819, SEC12830.

90. An internal signal diagram illustrates any timing or delays that occur during the triggering of a signal. Pathak, Tr. 991.

91. Timing was a critical factor in determining whether the erase command sequence proposed by Mr. Pathak, which was not disclosed in any Samsung documentation, was capable of causing Samsung 16M First Generation After Design Change product to perform multiblock erase. Pathak, Tr. 991; Thomas, Tr. 1548-1549.

92. Without an internal signal list and internal timing diagram, it is virtually impossible to determine the internal timing of signals within a device. Pathak, Tr. 991.

93. The internal signal list and internal timing diagram relating to the old designs of Samsung's 16M flash memory devices were important to Mr. Pathak's understanding of the operation of the circuit signals in the schematic. Pathak, Tr. 985-992.

94. Because there was no internal signal or timing documentation, access to the computer data base would enable SanDisk's expert, Jagdish Pathak, to come to a definitive determination regarding whether Samsung's new designs are capable of performing multiblock erase. Pathak, Tr. 985-992.

95. [[C]] Pathak, Tr. 681.

96. [[C]

] Pathak, Tr. 681.

97. [[C]

] Pathak, Tr. 700-701, 745-749; CX 45 at SEC33533-35.

98. [

] Pathak, Tr. 747-748, 876.

99. [[C]

] Pathak, Tr. 852-855.

100. [[C]

] Pathak, Tr. 853-855.

101. [[C]

] Pathak, Tr. 852-855.

102. [[C]

] Pathak, Tr. 861-865, 878-879.

103. [[C]] Choi, Tr. 1384-1386.

104. A net list would not enable an engineer to trace all the signals involved in a schematic. Pathak, Tr. 874-875.

105. [[C]] Thomas, Tr. 1479.

106. [[C]] Pathak, Tr. 870.

107. [[C]] Pathak, Tr. 870.

108. [ ] Pathak, Tr. 870-871.

109. [[C]] Pathak, Tr. 705-706.

110. [[C]] Thomas, Tr. 1475.

111. Mr. Pathak analogized his situation in analyzing Samsung's new designs to being sent to New York City, given a map where the street names are mislabeled and then told to find your way around. Pathak, Tr. 680-681.

112. The "Pathak Sequence" was not disclosed in the data book. Pathak Tr. 754.

113. [[C]] Pathak, Tr. 762-765.

114. [RESERVED]

115. [[C]] Pathak, Tr. 872-875.

116. [[C]] Pathak, Tr. 861-865, 878-879.

The `338 Patent

117. Samsung's flash memory devices are binary devices. CX 56 at 1151 (Samsung IEEE Journal article) ("In program operations, the page buffer latches are first serially loaded with program data: "0" for cells to be programmed and "1" for cells to be inhibited.").

118. Samsung's flash memory devices use a NAND architecture. CX 56 (Samsung IEEE Journal article).

119. Samsung's 4 Mbit, 16 Mbit, 32 Mbit and 64 Mbit flash memory devices operate in substantially the same way with respect to implementation of the `338 patent. Pathak, Tr. 789.

Samsung's Practice of the Preamble of Claim 27

120. Samsung's flash memory devices consist of "an array of addressable semiconductor electrically erasable and programmable memory (EEprom) cells on an integrated circuit chip" as recited in claim 27 of the `338 patent. Pathak, Tr. 789-790; CX 29 at Bates No. SEC 035132 (Samsung's 1996 data book).

121. Samsung's witnesses did not dispute that Samsung's flash memory devices consist of "an array of addressable semiconductor electrically erasable and programmable memory (EEprom) cells on an integrated circuit chip" as recited in claim 27 of the `338 patent. Tr. 464-465 (counsel).

122. Samsung's flash memory devices are "of the type having a source, a drain, [and] a control gate" as recited in claim 27 of the `338 patent. Pathak, Tr. 790-791; CX 43, Bates No. SEC 016352 (Samsung product literature).

Samsung's Practice of the "Erase Electrode" Element

123. Samsung's flash memory devices contain "an erase electrode" as that term is used in claim 27 of the `338 patent. Pathak, Tr. 790-791.

124. [[C]

] Pathak, Tr. 792-795; Thomas, Tr. 1579-1580; CX 56 at 1150-51 (Samsung IEEE Journal Article); CX 43C (Samsung product literature).

125. [[C]

] Pathak, Tr. 790-794.

126. [[C]

] Pathak, Tr. 792-795; Thomas, Tr. 1579-1580; CX 56 at 1150-51 (Samsung IEEE Journal Article); CX 43C (Samsung product literature).

127. [[C]

] Pathak, Tr. 794-794.

128. [[C]

]

Pathak, Tr. 792-795; Thomas, Tr. 1579-1580; CX 56 at 1150-51 (Samsung IEEE Journal Article); CX 43C (Samsung product literature).

129. [[C]

] Pathak, Tr. 794-794.

130. [[C]] Pathak, Tr. 792-795; Thomas, Tr. 1579-1580; CX 56, pp. 1150-51 (Samsung IEEE Journal Article); CX 43C (Samsung product literature).

131. [[C]] Pathak, Tr. 795.

Samsung's Practice of the Floating Gate Element

132. Samsung's flash memory devices contain "a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell," as recited in claim 27 of the `338 patent. Pathak, Tr. 795-796; CX 43 (Samsung product literature).

133. Samsung's witnesses did not dispute that Samsung's flash memory devices contain "a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell" as recited in claim 27 of the `338 patent. Thomas, Tr. 1462-1603.

Samsung's Practice of the Increment/Decrement Element

134. Samsung's flash memory devices satisfy the requirement of claim 27 that "a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions" as recited in claim 27 of the `338 patent. Pathak, Tr. 796-798; CX 52 (Samsung's programming algorithm); CX 56 (Samsung

IEEE Journal article).

135. [[C]

] Pathak, Tr. 796-798; CX 52 (Samsung's programming algorithm); CX 56 (Samsung IEEE Journal article).

136. [[C]

] Choi, Tr. 1351-1352.

137. Neither Mr. Thomas, Samsung's expert on whether SanDisk practices the '338 patent, nor any other Samsung witness offered any testimony to rebut Mr. Pathak's conclusion that Samsung's flash memory devices satisfy the limitation of claim 27 that "a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions." See Thomas, Tr. 1462-1604.

Samsung's Practice of the Temporary Storage Means

138. Samsung's flash memory devices perform the function of "temporarily storing a chunk of data for programming a plurality of addressed cells." Pathak, Tr. 798-805.

139. [[C]

] CX 56 at 1151 (Samsung IEEE Journal article) [[C]

] Pathak, Tr. 803-804 [[C]

]CPX 59.

140. [[C]] CX 56 at 1151 (Samsung IEEE Journal article) [[C]]; CPX 128, line 2.

141. [[C]] Thomas, Tr. 1584-1585.

142. [[C]] Pathak, Tr. 799-802; CX 46 (Samsung core schematics); CX 56 at 1150-51 (Samsung IEEE Journal article); CPX 57C; CPX 63C (modification of Samsung core schematic).

143. [[C]] Pathak, Tr. 802-803; CX 2 ('338 Patent), Fig. 5; CX 56 at 1150 (Samsung IEEE Journal article); CPX 59C.

144. [[C]] Pathak, Tr. 804-805.

Samsung's Practice of the Parallel Programming Means

145. Samsung's flash memory devices perform the function of "programming in parallel the stored chunk of data into the plurality of addressed cells." Pathak, Tr. 805-808.

146. [[C]

] Thomas, Tr. 1590-1591.

147. [[C]

] Pathak, Tr. 805-808; CX 46C (Samsung core schematic); CPX 61C.

148. [[C]

] Pathak, Tr. 808; Mehrotra, Tr 337.

149. [[C]

] Pathak, Tr. 808-812; Mehrotra, Tr. 336.

150. [[C]

] Pathak, Tr. 808-813; CPX 137-139.

151. [[C]

] Mehrotra, Tr. 336-338; Pathak, Tr. 808-813; CPX 137-139.

Samsung's Practice of the Verification Means

152. Samsung's flash memory devices perform the function of "verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data." Pathak, Tr. 814-81; CPX 60.

153. [[C]

] Thomas, Tr. 1594-1595; RX 15C at 49 (Expert Report of Mammen Thomas).

154. [[C]

]

Choi, Tr. 1409-1410; CX 56 at 1154 (Samsung IEEE Journal article).

155. [[C]

] Pathak, Tr. 818-819; CX 48C (Samsung 16 MBit NAND functional block diagram); CPX 60C.

156. [[C]

] RX 15C at 49 (Expert Report of Mammen Thomas).

157. [[C]

] Pathak, Tr. 814-820, 829-831, 959-960, 975; RX 205 at 15 (Expert Report of Jagdish Pathak); CX 48C (Samsung 16 MBit functional block diagram); CPX 60C; CPX 127.

158. A flash prom cell must be erased before it can be programmed or reprogrammed. Pathak, Tr. 932-933; CX 2 at col.1, lines 46-54, and col.

19, lines 60-63.

159. [[C]] Choi, Tr. 1354-1356.

160. The `338 patent discloses that "if each memory cell is to store K states, then at least K-1, or preferably K reference levels need be provided." CX 2 at col. 11, lines 56-58.

161. The `338 patent discloses that in a two-state implementation, only a single reference level is required. CX 2 at col. 11, lines 56-58.

162. The '344 patent, which is incorporated by reference into the `338 patent, discloses that to sense the correct one of K states, only K-1 reference levels and K-1 sense amplifiers are required. CX 3 ('344 Patent) at col. 26, lines 51-55.

163. The '344 patent, which is incorporated by reference into the `338 patent, expressly discloses that a single sense amplifier and a single reference level can be used to differentiate between conduction states "1" (e.g., or programmed) and "0" (e.g., or erased). CX 3 ('344 Patent) at col. 26, lines 55-60.

164. The '344 patent, which is incorporated by reference into the `338 patent, expressly states that Figure 11-E can be implemented using a single sense amplifier. CX 3 ('39644 Patent) at col. 26, lines 8-15.

165. The '344 patent, which is incorporated by reference into the `338 patent, explicitly discloses that "the same principle employed in the circuit of Figure 11-E can be used also with binary storage." CX 3 ('344 Patent) at col. 26, lines 66-67.

Samsung's Practice of the Inhibit Means

166. Samsung's flash memory devices perform the function of "inhibiting further programming of correctly verified cells among the plurality of

addressed cells." Pathak, Tr. 833-835; CPX 62C.

167. [[C]

] Thomas, Tr. 1597.

168. [[C]

] Pathak, Tr. 833-835; CPX 62C.

169. [[C]

] Pathak, Tr. 833-835, 840-841; CPX 62C, 123, 127.

170. [[C]

] Pathak, Tr. 833-835; CPX 62C.

171. The Samsung flash memory device performs the function of "inhibiting further programming of "correctly verified" cells among the plurality of addressed cells" in an equivalent manner to that disclosed in the `338 patent. Pathak, Tr. 967-969.

172. Dr. McGreivy testified that terminating programming of verified cells will improve the performance of a binary device and prevent it from wearing out a little earlier and is needed in a multi-level device to prevent misprogramming of data. McGreivy, Tr. 1697-1701, 1797-1799.

173. Samsung's devices perform the function of inhibiting further programming of a "correctly verified" cell, until all cells in the chunk have been verified. Pathak, Tr. 842-845; Thomas, Tr. 1597.

174. [[C]

] Pathak, Tr. 840-841 (equating Samsung's page buffer latch with latch 721 disclosed in the patent); CX 56 at 1151, col. 2, lines 21-23); CPX 123 (simplified Samsung verification circuit); CPX 53 (showing Samsung's verification circuit in more detail); CX 56, Fig. 1 (Samsung publication describing the inhibiting scheme); CX 46 C (showing Samsung's most detailed core schematics); Pathak, Tr. 845-846 (equating simplified Samsung circuits to features in core schematics).

175. [[C]] CPX 60 C (described at Pathak, Tr. 842-843; CX 56 at 1152, Fig. 5(a); Thomas, Tr. 1519.

176. [[C]] CX 56 at 1153, col. 1, lines 2-12; Thomas, Tr. 1119-1120.

177. Flipping the latch 721 disclosed in the `338 patent flips causes 0 volts to be applied to the drain of the disclosed NOR cell. Mehrotra, Tr. 332, 352-353; Pathak, Tr. 967.

178. Although the latch 721 in the `338 patent outputs a logical "1" in the non-verified state while [[C]](compare CX 2, Col. 20 with CPX 60-C) these differences are insubstantial given that each signal will inhibit programming in its respective NAND or NOR architecture (see Mehrotra, Tr. 338-339) and that

FIG. 16 of the '338 patent includes an inverter 723 which could be removed to provide the logical output required by Samsung (CX 2).

Samsung's Practice of the Final Means of Claim 27

179. Samsung's flash memory devices perform the function of "further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of "correctly verified" cells until all the plurality of addressed cells are verified correctly." Pathak, Tr. 841-846; CX 46C (Samsung core schematic); CPX 60, 62.

180. [[C]

] Pathak, Tr. 844-845.

181. [[C]

] Pathak, Tr. 841-846; CX 46C (Samsung core schematic); CPX 60, 62.

182. [[C]

] Pathak, Tr. 841-846; CX 46C (Samsung core schematic); CPX 60, 62.

183. Neither Samsung's Pre-Hearing Statement nor the hearing testimony of Samsung's infringement expert, Mr. Thomas, disputes that if Samsung's

devices fall within the scope of the verify means and the inhibit means, they also satisfy the final claim 27 means plus function element. Respondents' Post-Hearing Br.; Thomas, Tr. 1462-1604.

VI. DOMESTIC INDUSTRY

A. Economic Requirements

1. During the course of trial, Respondents conceded that Complainant SanDisk's domestic activities satisfy the economic prong of the domestic industry requirement. Tr. 657-659.

2. SanDisk produces and sells (1) flash memory cards; (2) flash drive products that emulate small form factor drive products; (3) compact flash products (each of which contain flash EEPROMs that are covered by the '752 and '338 patents); and (4) flash EEPROM chip sets. Auclair, Tr. 628.

3. Every flash memory card produced and sold by SanDisk incorporates a controller. Harari, Tr. 110.

4. Every flash drive produced and sold by SanDisk incorporates a controller. Harari, Tr. 112-113.

Domestic Production

5. With the exception of wafer production, virtually all of the activities related to the production of SanDisk's memory products take place in the United States. Auclair, Tr. 621.

6. SanDisk sold over $[[C]] worth of its 16 and 32 Mbit flash memories products in 1995. CX 78C.

7. SanDisk sold approximately $62 million dollars worth of its 16 and 32 Mbit flash memory products in 1995. Harari, Tr. 138.

8. In 1994 and 1995, respectively, SanDisk spent approximately $[[C]] and $[[C]]on manufacturing and testing expenses. CX 69C.

9. SanDisk spent approximately $[[C]]on manufacturing and testing expenses in the first half of 1996. Auclair, Tr. 653.

10. SanDisk's domestic activities in relation to its flash memory products

are sufficient to authorize it under the applicable regulations to affix a "Made in the USA" designation to its products. Auclair, Tr. 657-658.

Plant and Equipment

11. SanDisk leases a [[C]] square foot facility in Santa Clara, California, which serves as its corporate headquarters, and its research, development, marketing, and product support facility. SanDisk also leases a nearby building where it conducts product testing, shipping and receiving, and certain manufacturing related activities. CX 65C.

12. SanDisk purchased [[C]]machines for testing its wafers at a cost of approximately $[[C]]each. Auclair, Tr. 631.

Labor or Capital

13. As of the time of the hearing, [C] members of SanDisk's labor force were directly involved in manufacturing activities related to flash memory products. Auclair, Tr. 621.

14. [[C]

] Auclair, Tr. 622-623, 631, 644.

Research and Development

15. SanDisk has spent over $[[C]]on research and development in the United States related to flash memory products allegedly covered by the '752 and '338 patents since 1990. [[C]

] Auclair, Tr. 640-643.

16. [[C]

] Harari, Tr. 184;

Auclair, Tr. 618-619, 629.

17. [[C]

] Harari, Tr. 185.

18. [[C]

] Harari, Tr. 94, 184;

Auclair, Tr. 639- 649.

19. SanDisk has licensed Intel to practice the patents at issue. Harari, Tr. 281; CX 115C.

20. [[C]

] Harari, Tr. 283-284; CX 115C.

21. [[C]

] Harari, Tr. 284-285.

B. Technical Requirements

The `752 Patent

22. Claims 1, 2 and 4 of the `752 patent are incorporated into every product SanDisk has ever sold -- its 4 Mbit, 8 Mbit, 16 Mbit and 32 Mbit devices. See Guterman, Tr. 437-438.

23. The `752 patent is based on the SanDisk inventors' work in developing SanDisk's first flash memory products. Harari, Tr. 35-39; CX 12C at 71990.

24. [[C]

] CX 21C at 9.

25. [[C]] CX 21C at 9.

26. [[C]] CX 21C at 9.

27. [[C]] CX 21C at 9; CPX 53C.

28. SanDisk's devices possess "one or more integrated circuit chips each having an array of Flash EEprom cells partitioned into a plurality of sectors, each sector addressable for erase such that all cells therein are erasable simultaneously." Guterman, Tr. 443-447.

29. In its Prehearing Statement, Samsung did not address the issue of whether SanDisk's devices possess the first element of claim 1. Respondents' Post-Hearing Br. at 98-100.

30. [[C]] Guterman, Tr. 444-445; CX 21C at 7; CPX 16.

31. [[C]] CX 21C at 7.

32. [[C]] CX 21C.

33. [[C]] Guterman, Tr. 439-441; CX 21C; CPX 51C; CPX 53C; CPX 54C.

34. SanDisk's devices possess a "means for selecting a plurality of sectors" as claimed in the `752 patent. Guterman, Tr. 457-458.

35. SanDisk's devices perform the function of "selecting a plurality of sectors for erase." Guterman, Tr. 439-442, 457-458; CX 21C at 9; CPX 51C; CPX 53C; CPX 54C.

36. [[C]

] See Guterman, Tr. 456-459; CX 21C at 9; CPX 49C; CPX 50C; CPX 51C.

37. There is no structure in the `752 patent that is used to permanently designate a fixed plurality of sectors for erase. See CX 1.

38. [[C]

]

Guterman, Tr. 439-442; CX 21C at 9; CPX 51C; CPX 53C; and CPX 54C.

39. [[C]

] Guterman, Tr. 439-442; CX 21C at 9; CPX 51C; CPX 53C; and CPX 54C.

40. SanDisk's devices possess a "means for simultaneously performing the erase operation on only the ... selected sectors." See Guterman, Tr. 459-460.

41. [[C]

] Guterman, Tr. 459-460; CPX 81.

42. [[C]

] CX

21C at 9.

43. SanDisk's devices possess an individual register associated with each sector as described in claim 1 of the '752 patent. Guterman, Tr. 556-557; CPX 51C.

44. [[C]

]

45. [[C]

] Guterman, Tr. 453-456, 542; CX 21C at 9; CPX 50C; and CPX 54C.

46. [[C]

] Thomas, Tr. 1576.

47. [[C]

] Thomas, Tr. 1572-1575; CPX 81A.

48. [[C]

] See Guterman, Tr. 543, 556-557; CPX 51C.

49. [[C]

]

50. [[C]

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51. [[C]

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52. [[C]

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53. [[C]

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54. [[C]

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55. [

]

56. SanDisk's individual register produces the same result as the register disclosed in the '752 patent. It holds a status to indicate whether its associated sector is selected or not. Guterman, Tr. 453-457; CX 21C.

57. The "simultaneously erasing means" in SanDisk's flash memory devices is "responsive to the status in each of the individual registers, such that only the selected sectors are included in the erasing." Guterman, Tr. 462.

58. [[C]

]

59. SanDisk's flash memory devices satisfy the requirement of claim 4 that: "all of the individual registers are simultaneously resettable to a status indicating the associated sectors as not selected." See Guterman, Tr. 463.

60. [[C]

]

61. [[C]

]

The `338 Patent

62. [[C]

] Guterman, Tr. 517.

SanDisk's Practice of the Claim 27 Preamble

63. Samsung stipulated at the hearing that SanDisk's flash memory devices consist of "an array of addressable semiconductor electrically erasable and programmable memory (EEprom) cells on an integrated circuit chip, the memory cell being of the type having a source, a drain, [and] a control gate" as recited in claim 27 of the `338 patent. Tr. 464-465; CX 2 at col. 26.

SanDisk's Practice of the "Erase Electrode" Element

64. [

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65. Samsung stipulated at the hearing that SanDisk's flash memory devices

have "an erase electrode receptive to specific voltage conditions" as recited in claim 27 of the '338 patent. Tr. 464-465; CX 2 at 26, lines 28-36.

SanDisk's Practice of the Claim 27 "Floating Gate" Element

66. Samsung stipulated at the hearing that SanDisk's flash memory devices contain "a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell." Tr. 464-465; CX 2 at col. 26, lines 28-36.

SanDisk's Practice of the Claim 27 Increment/Decrement Element

67. SanDisk's flash memory devices satisfy the requirement of claim 27 that "a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions" as recited in claim 27 of the `338 patent. See Guterman, Tr. 472-474, 566-567.

68. [[C]

69.

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SanDisk's Practice of Claim 27 Temporary Storage Means

71. SanDisk's flash memory devices perform the function of "temporarily storing a chunk of data for programming a plurality of addressed cells." See Guterman, Tr. 474-483, 581.

72. In the SanDisk flash memory devices, [[C]

73.

74.

75.

76.

77.

]

SanDisk's Practice of Claim 27 Parallel Programming Means

78. SanDisk's flash memory devices perform the function of "programming in parallel the stored chunk of data into the plurality of addressed cells." Guterman, Tr. 483-486; CX 23C at Bates No. SD005815 (SanDisk schematics).

79. SanDisk's flash memory devices perform the parallel programming function [[C]

80.

81.

]

SanDisk's Practice of Claim 27 Verification Means

82. SanDisk's flash memory devices perform the function of "verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data." Guterman, Tr. 486-488; CX 23C (SanDisk schematics).

83. [

84.

85.

86.

87.

88.

]

SanDisk's Practice of Claim 27 Inhibit Means

89. SanDisk's flash memory devices perform the function of "inhibiting further programming of "correctly verified" cells among the plurality of addressed cells." See Guterman, Tr. 504-513; CX 23C (SanDisk circuit schematics).

90. SanDisk's flash memory devices [

[C]

SanDisk's Practice of Claim 27 Final Means

91. SanDisk's flash memory devices perform the function of "further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of "correctly verified" cells until all the plurality of addressed cells are verified correctly." Guterman, Tr. 513-517; CX 23C (SanDisk circuit schematics).

92. SanDisk's flash memory devices [

[C]

93.

94.

]

CONCLUSIONS OF LAW

1. The Commission has personal jurisdiction over the parties and subject matter jurisdiction over this investigation. See Op. at 2.

2. There have been importations and sales after importation of accused products. See Op. at 11.

3. It has not been demonstrated by clear and convincing evidence that claims 1, 2 and 4 of the `752 patent are invalid. See Op. at 81, 85, 90, 92.

4. It has not been demonstrated by clear and convincing evidence that claim 27 of the `338 patent is invalid. See Op. at 93, 96, 99, 102.

5. Respondents literally infringe claims 1, 2 and 4 of the `752 patent. Alternatively, Respondents infringe under the doctrine of equivalents. See Op. at 107, 110-12.

6. Respondents literally infringe claim 27 of the `338 patent literally. Alternatively, Respondents infringe under the doctrine of equivalents. See Op. 128.

7. Complainant's investments and activities with respect to the `752 and `338 patents satisfy the domestic industry requirement of section 337. See Op. at 129, 136-41.

8. There is a violation of section 337(a)(1)(B) with respect to the `752 patent and the `338 patent. See Conclusions of Law 1-7.

INITIAL DETERMINATION AND ORDER

Based on the foregoing opinion, findings of fact, conclusions of law, the evidence, and the record as a whole, and having considered all pleadings and arguments as well as proposed findings of fact and conclusions of law, it is the Administrative Law Judge's INITIAL DETERMINATION ("ID") that a violation of § 337 exists in the importation and sale of certain flash memory circuits and products containing same by reason of infringement of claims 1, 2 and 4 of U.S. Letters Patent 5,418,752 and claim 27 of U.S. Letters Patent 5,172,338.

The Administrative Law Judge hereby CERTIFIES to the Commission this ID, together with the record of the hearing in this investigation consisting of the following:

1. The transcript of the hearing, with appropriate corrections as may hereafter be ordered by the Administrative Law Judge; and further

2. The exhibits accepted into evidence in this investigation as listed in the attached exhibit lists.

In accordance with 19 C.F.R. § 210.39(c), all material found to be confidential by the Administrative Law Judge under 19 C.F.R. § 210.5 is to be given in camera treatment.

The Secretary shall serve a public version of this ID upon all parties of record and the confidential version upon counsel who are signatories to the Protective Order issued by the Administrative Law Judge in this investigation, and the Commission Investigative Attorney. To expedite service of the public version, counsel are hereby ordered to serve on the Administrative Law Judge by no later than March 5, 1997, a copy of this ID with those sections considered by the party to be confidential bracketed in red.

Pursuant to 19 C.F.R. § 210.42(h), this ID shall become the determination of the Commission unless a party files a petition for review pursuant to § 210.43(a) or the Commission, pursuant to § 210.44, orders on its own motion a review of the ID or certain issues herein.

Sidney Harris
Administrative Law Judge

Issued: February 26, 1997

CERTAIN FLASH MEMORY CIRCUITS
AND PRODUCTS CONTAINING SAME

INV. NO. 337-TA-382

CERTIFICATE OF SERVICE

I, Donna R. Koehnke, hereby certify that the attached Initial Determination [Public] was served upon Juan Cockburn, Esq. and upon the following parties via first class mail, and air mail where necessary, on March 26, , 1997.

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CERTIFICATE OF SERVICE--Continued

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